SGM41573 Demo Board Test Report

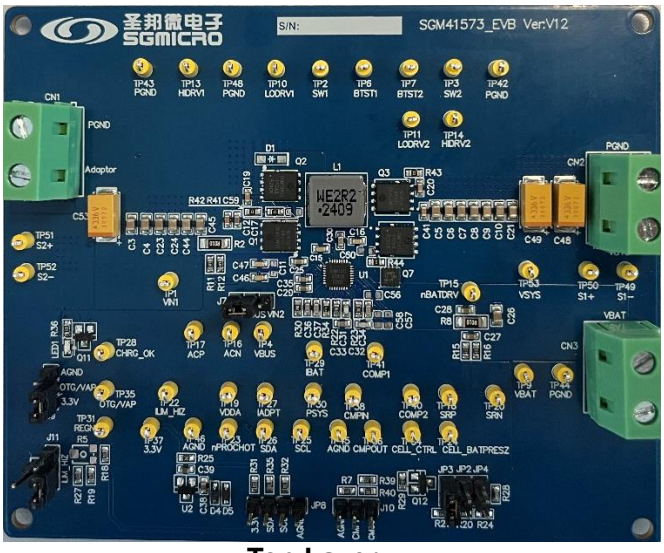
I²C Controlled, 1-4 Cells, Buck-Boost Battery Charger with NVDC Power Path Management

Input Voltage Range: 3.6V to 24V

Battery Cells Range: 1-4 Cells

Charge Current Range: 0A to 8.128A

Demo Board Picture:



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1. Demo Board User's Guide

1.1 Demo Board Features

The SGM41573 demo board is a complete charger module for evaluating the I²C-controlled, 1-4 cells Buck-Boost battery charger in TQFN-4×4-32AL package. It has below key features:

- 1- to 4-Cell Charging from a Variety of Input Types
  - 3.6V to 24V Input Operating Voltage Range
  - USB 2.0/3.0/3.1 (Type C)/USB-PD Input Current Support
  - Seamless Buck ↔ Buck-Boost ↔ Boost Transitions
  - Input Overload Protection (IDPM and VDPM Regulation)
- CPU Throttling, Power and Current Monitoring
  - Full nPROCHOT Profile
  - Input Current Monitoring
  - Battery Charge/Discharge Current Monitoring
  - System Power Monitoring
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with Depleted or No Battery
  - Battery Supplementation if Adapter is Fully Loaded
  - BATFET Ideal Diode Emulation in Supplement Mode
- Power-Up USB Port from Battery (USB OTG)
  - 3V to 20.56V Adjustable OTG Voltage with 8mV Resolution
  - Up to 6.35A Output Current Limit with 50mA Resolution
- 800kHz or 1.2MHz Selectable Switching Frequency

Note: This demo board does not include the SGM USB dongle board.

Table 1 lists the recommended operating conditions for the demo board.

Table 1. Recommended Operation Conditions

Parameters	Range
The Input Voltage Range in Forward Mode	3.6V to 24V, typical 5V/9V/12V/20V
Battery Voltage in Forward Mode	0V to 19.2V (or floating), typical 12.6V for 3-cell
Battery Voltage in OTG Mode	3.6V to 19.2V, typical 12.6V for 3-cell
The Output Voltage Range in OTG Mode	3V to 20.56V, default 4.28V
Fast Charging Current	0A to 8.128A (64mA step)
Input Current Limit in Forward Mode	50mA to 6.35A
Output Current Limit in OTG Mode	0A to 6.35A
Operating Ambient Temperature Range	-40℃ to +85℃

1.2 Test Setup

1.2.1 Forward Mode

1.2.1.1 Demo Board Setup

The following illustration is based on an example of 3-cell battery charging.

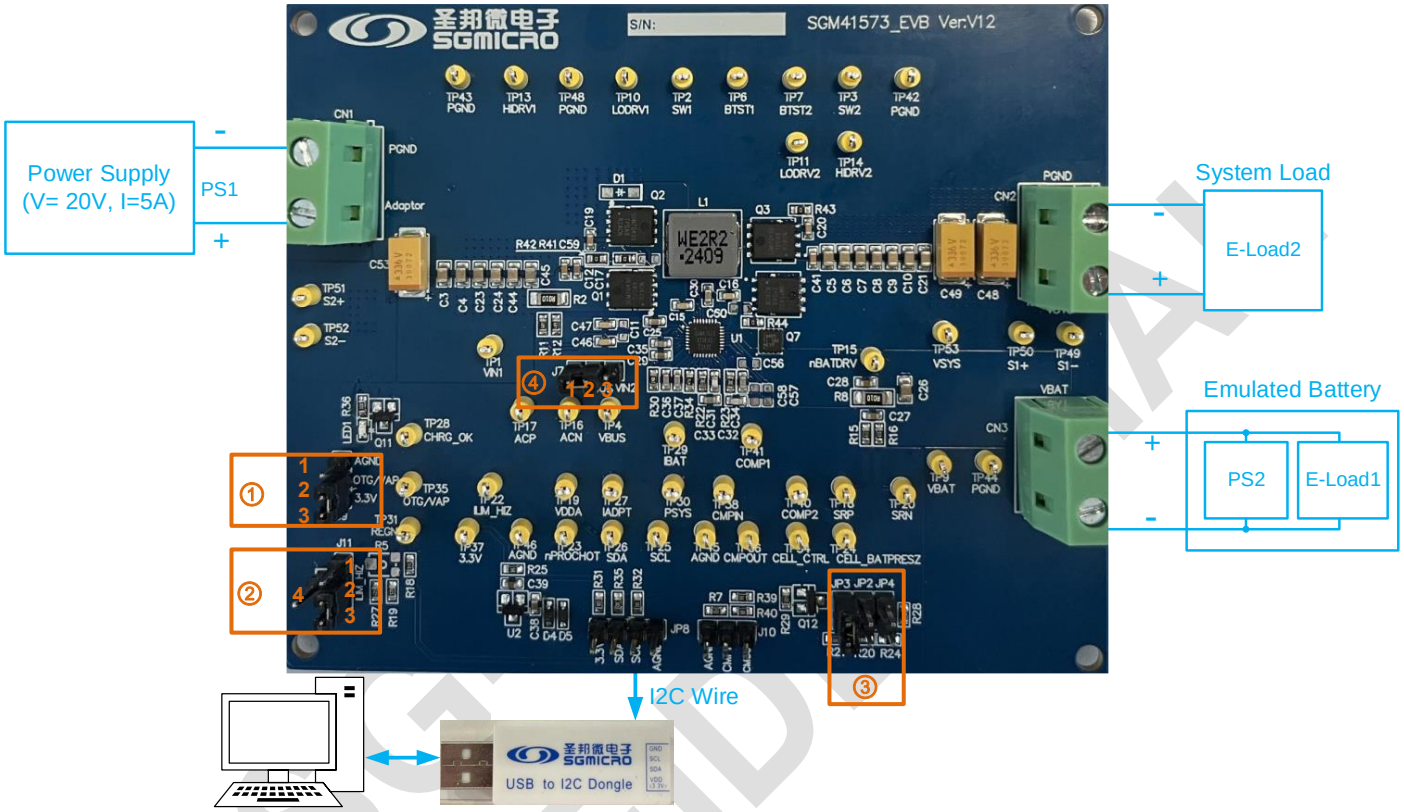


Fig-1: SGM41573 Demo Board Setup in Forward Mode

A. Equipment and Connection

1. The equipment required in this test include:
   a. PS1 set to 20V with 5A current limit (larger than default IINDPM limit).
   b. PS2 set to 12V/5A with a parallel E-load1 (load 4A) to emulate battery.
   c. The E-load2 for the system load.
   d. An USB dongle and PC.

   Note: The emulated battery also can be replaced by a real battery.

B. Connection of Jumper Cap

Table 2 displays the connection of jumper cap. The corresponding positions and PIN are shown in Fig-1.

Table 2. Connection of Jumper Cap

Header	Description	Connection
J9	OTG or VAP Modes enable setting: 1. Pull high (connect PIN2 and PIN3): enable OTG or VAP Modes 2. Pull low (connect PIN1 and PIN2): disable OTG or VAP Modes	Connect PIN 2 and PIN 3 of J9
J11	External current limit and external HIZ Mode setting: 1. Connect PIN2 and PIN3: through a resistor divider between supply and ground to set the target input current limit 2. Connect PIN2 and PIN4: entre HIZ MODE	Connect PIN 2 and PIN 3 of J11
JP2 JP3 JP4	CELL setting: 1S: JP2, JP3, JP4 open 2S: only JP2 short 3S: only JP3 short 4S: only JP4 open Battery removal: only JP4 short	Only JP3 short
J7	VBUS power supply setting: 1. Connect PIN1 and PIN2: VBUS is powered by VIN 2. Connect PIN2 and PIN3: VBUS is powered by VIN2	Connect PIN1 and PIN2 of J7

C. Connection Steps of Main Circuit

1) Connect the PS1 (20V/5A) to the demo board between Adaptor and PGND which is shown in Fig-1.

2) Connect the emulated battery (PS1 set to 12V/5A and E-load1 set to 4A load) to the demo board between VBAT and PGND which is shown in Fig-1.

3) Connect the E-load2 between VSYS and PGND which is shown in Fig-1.

4) Turn on the emulated battery, PS1 and E-load2 in turn.

1.2.1.2 I²C Register Setup

1. After hardware setup done as shown in *1.2.1.1*, connect the USB dongle to PC, then open the SGM USB GUI interface as Fig-2, choose the “SGM41573” and click “Entry” button to entry the GUI interface.

Fig-2: SGM USB GUI Interface

2. After entry the SGM41573 GUI interface as shown in Fig-3, the bottom left corner of the page will display “USB-to-I2C Dongle has been plugged in!” firstly, then click the “Read All” button, if "Device ACK" is displayed, it means the I²C communication is normal.

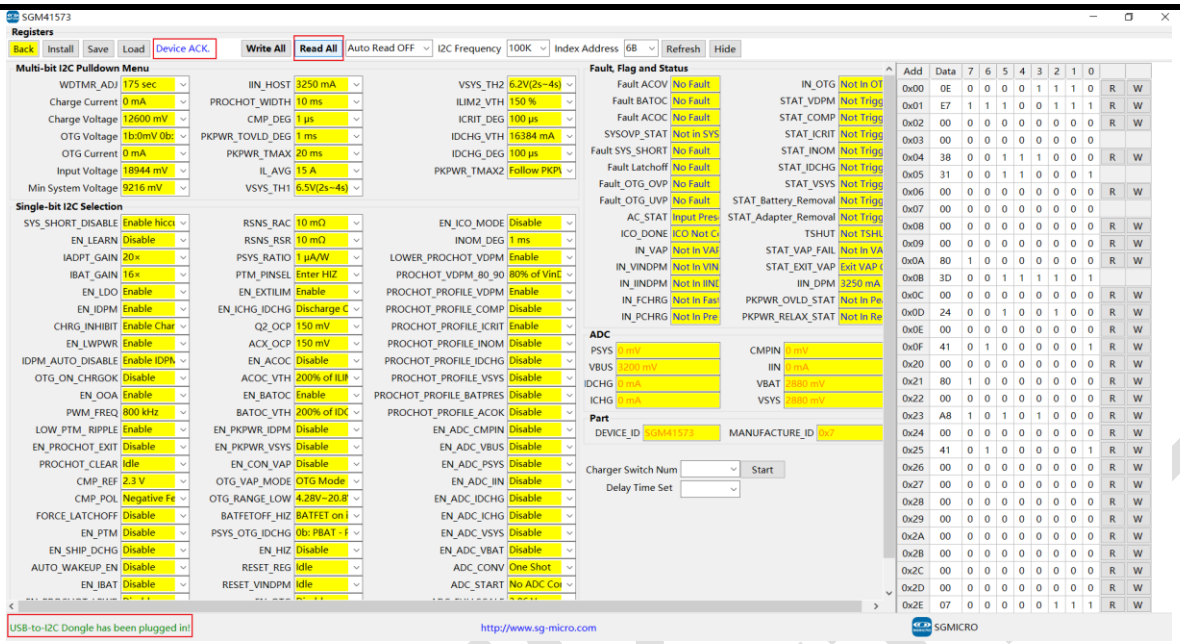


Fig-3: SGM41573 GUI Interface

3. After both the hardware and software setup done, the registers can be read/written normally according to the test. Ensure/change the registers setting as following (for an example of 3-cell battery fast charge):

1) Disable the Watchdog Timer (REG0x01[6:5] = 00).

2) Set the charge current to 3A (REG0x02[7:6] = 11, REG0x03[4:0] = 01011).

3) Disable the EXTILIM (REG0x32[7] = 0).

4) Click "Read All", then you will find the IN_FRCHRG Status is "In Fast Charge" and the charge current is 3A.

Note: Under 3-cell battery condition, the Charge Voltage is setting to 12600mV in default, the Min System Voltage is setting to 9216mV, the Input Voltage (VINDPM) is auto setting to VIN-1.28V. Users can change the connection of CELL_BATPRESZ PIN to modify default configuration. Below GUI interface screenshot is for reference.

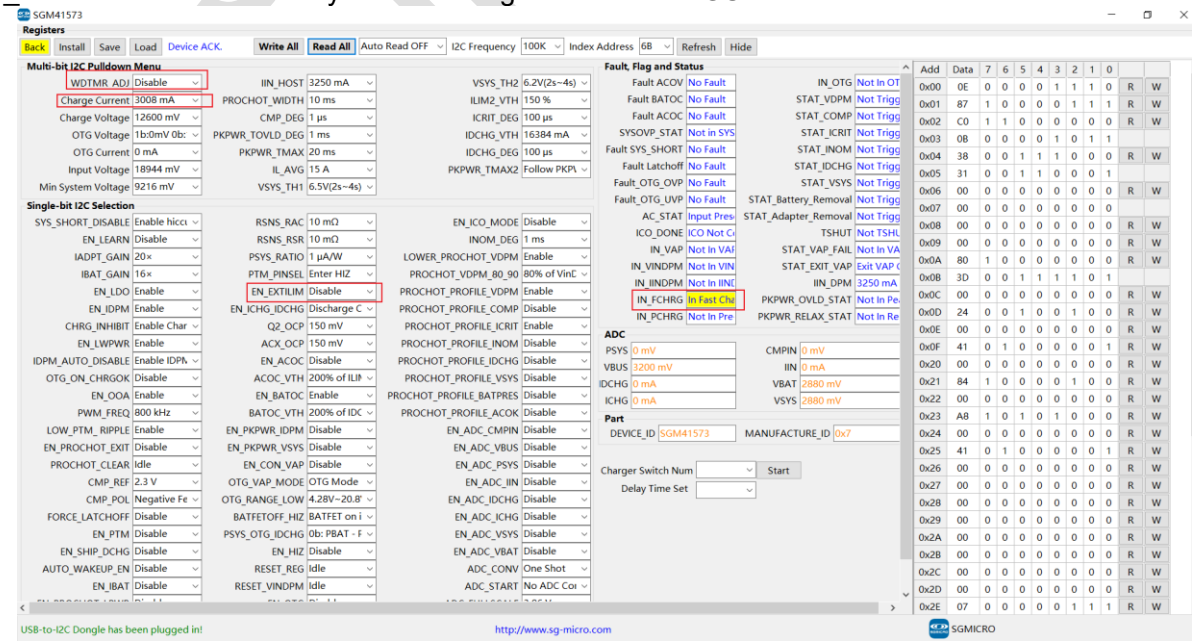


Fig-4: SGM41573 register setting for an example of 3-cell battery charging

1.2.1.3 Test Procedure

After both hardware and software setup done as shown in *1.2.1.1* and *1.2.1.2*. The SGM41573 forward charging mode is enabled. Follow Fig-5 and below steps for demo board forward charging mode measurement and verification:

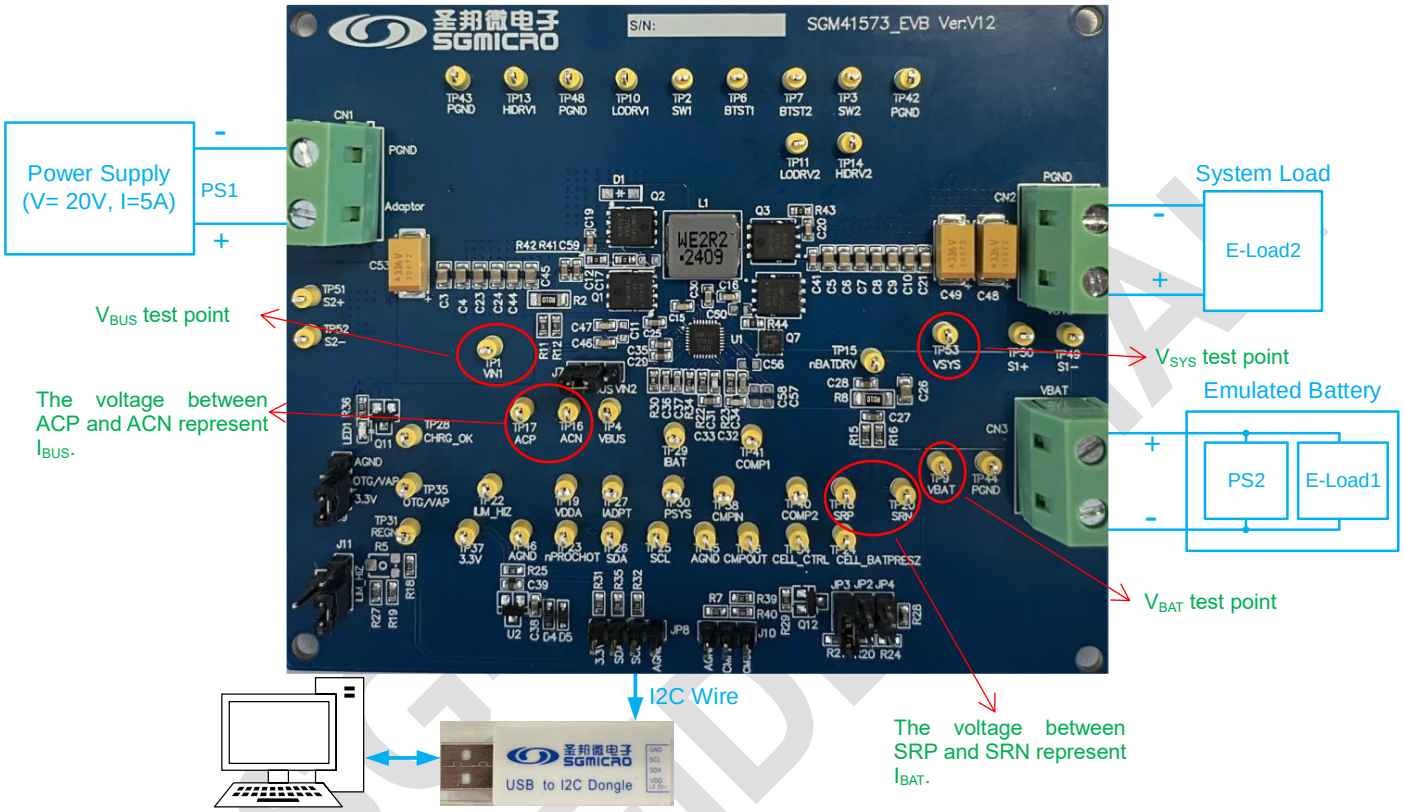


Fig-5: SGM41573 Demo Board Forward Mode Test Measurement

1. When the SGM41573 enters forward mode, the V_{BUS}, V_{SYS}, V_{BAT}, I_{BUS}, I_{BAT} can all be measured.

2. The current sense resistor R2, R8 are 10mΩ, and the ACP/ACN, SRP/SRN measure the sense resistor voltage to give the IBUS and IBAT, respectively.

3. Optional, in this setup, change the power supply voltage or I^2C register setting can observe the SGM41573 other features as following. During the test, the corresponding STAT and FLAG registers are helpful to judge the IC operation status.

   a. Change the emulated battery voltage can observe different charge phase and VBAT_OVP behavior.
   b. Change the input power supply voltage can observe the VBUS_OVP behavior.
   c. Change the system voltage can observe the VSYS_OVP behavior.
   d. Short the SYS and PGND can observe the SYS_SHORT behavior.
   e. Enable EN_BATOC (REG0x32[1]) , set IDCHG_VTH (REG0x39[7:2]) and IDCHG_DEG (REG0x39[1:0]) can observe the BATOC behavior.
   f. Increase the system load to trigger IINDPM/VINDPM regulation and enter supplement mode.
   g. Enable/disable charge by I^2C register (REG0x00[0]).
   h. Other protections.

4. Optional, when the ADC function is tested, enable EN_ADC register and set ADC_START register to Start ADC Conversion, then observe the ADC value.

1.2.2 OTG Mode

1.2.2.1 Demo Board Setup

The demo board setting is the same as *1.2.1.1* chapter, except the connection of Adaptor change from PS1 to E-load3, which is shown in Fig-6. Please refer to Chapter *1.2.1.1* for details.

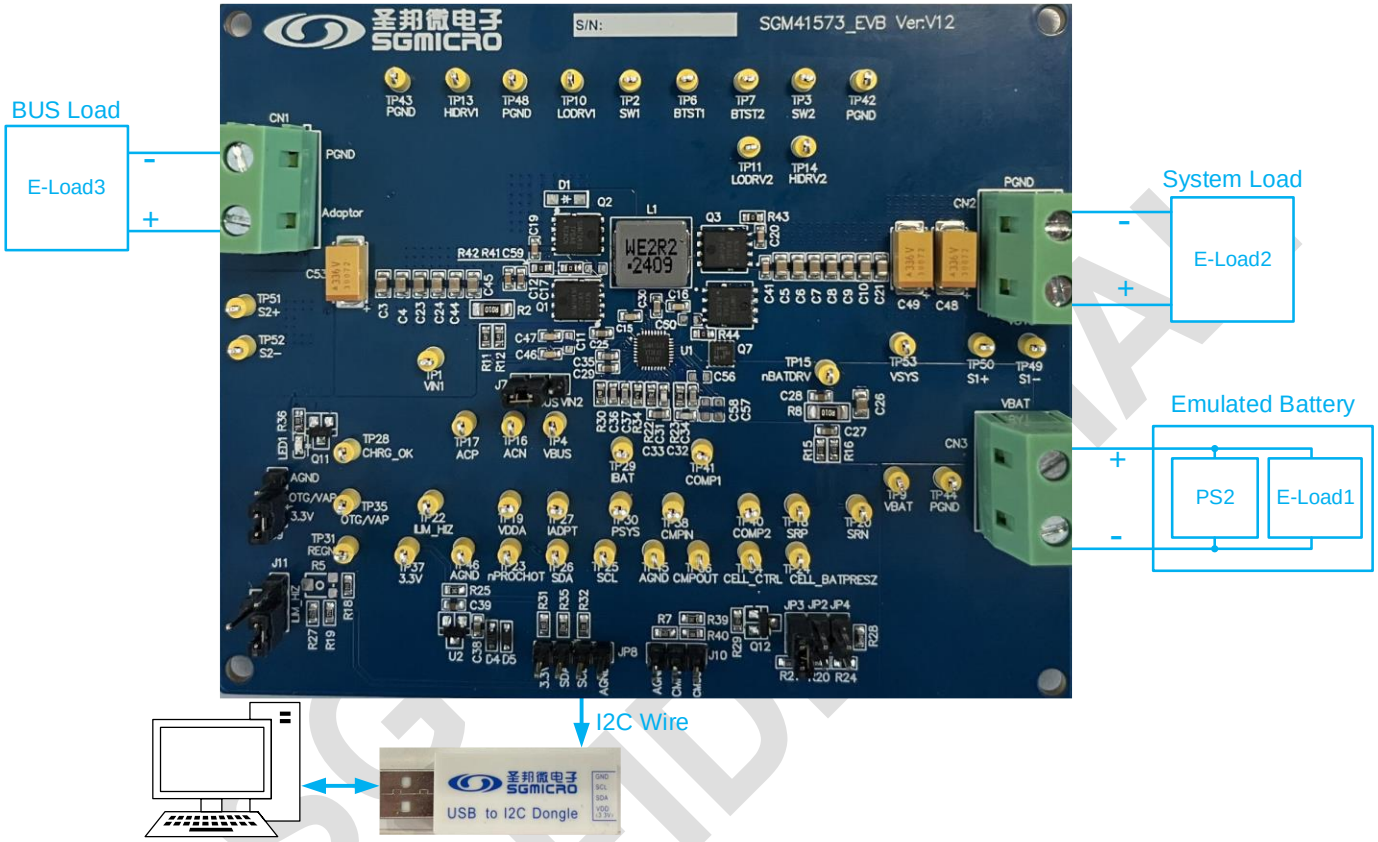


Fig-6: SGM41573 Demo Board Setup in OTG Mode

1.2.2.2 I²C Register Setup

After hardware setup done as shown in *1.2.2.1*, open the SGM41573 GUI (refer to *1.2.1.2*), ensure/change the registers setting as following (for an example of 3-cell battery):

1. Disable the Watchdog Timer (REG0x01[6:5] = 00).
2. Disable HIZ mode (default, REG0x35[7] = 0).
3. OTG Voltage = 5V (REG0x06[7:2] = 010001; REG0x07[5:0] = 000111).
4. OTG Current = 5A (REG0x09[6:0] = 1100100).
5. OTG_VAP_MODE = OTG MODE (default, REG0x34[5] = 1).
6. Enable OTG mode (REG0x35[4] = 1).

Below GUI Interface screenshot is for reference. (The purple wireframe displays the OTG status)

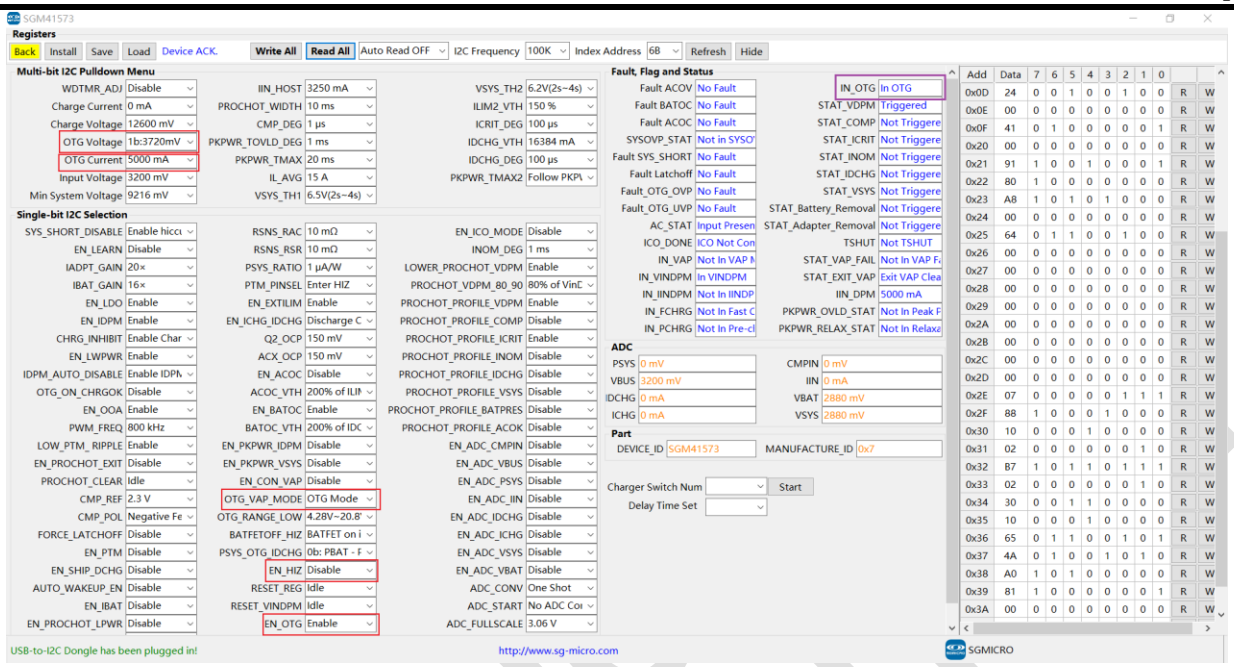


Fig-7: SGM41573 register setting example in OTG mode

1.2.2.3 Test Procedure

After both hardware and software setup done as shown in *1.2.2.1* and *1.2.2.2*, The SGM41573 OTG mode is enabled. Follow Fig-8 and below steps for demo board OTG mode measurement and verification:

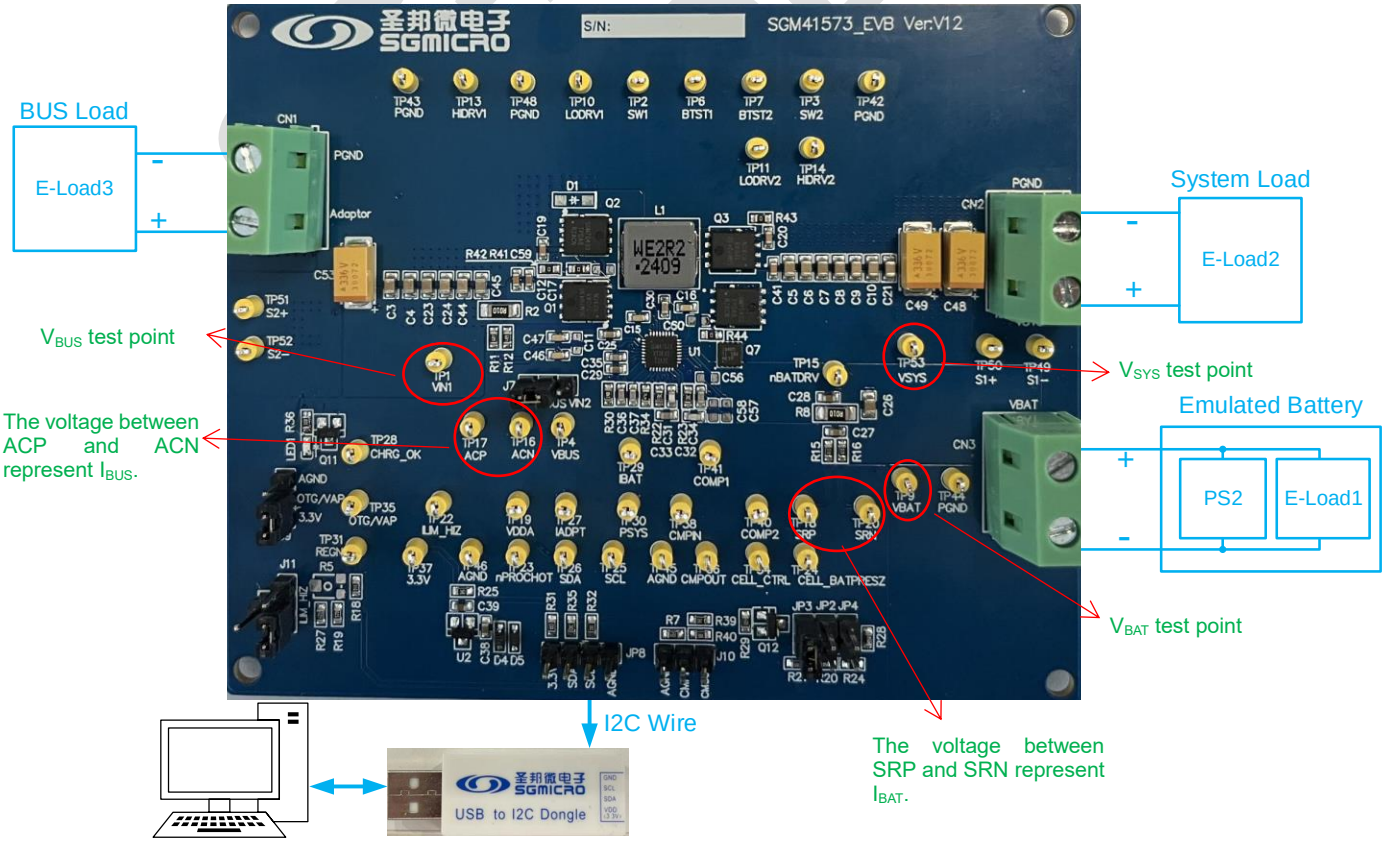


Fig-8: SGM41573 Demo Board OTG Mode Test Measurement

1. When the SGM41573 enters OTG mode, the V_{BUS}, V_{SYS}, V_{BAT}, I_{BUS}, I_{BAT} can all be measured.

2. The current sense resistor R2, R8 are 10mΩ, and the ACP/ACN, SRP/SRN measure the sense resistor voltage to give the I_{BUS} and I_{BAT}, respectively.

3. Optional, in this setup, change the OTG output load or I^2C register setting can observe the SGM41573 other features as following. During the test, the corresponding STAT and FLAG registers are helpful to judge the IC operation status.

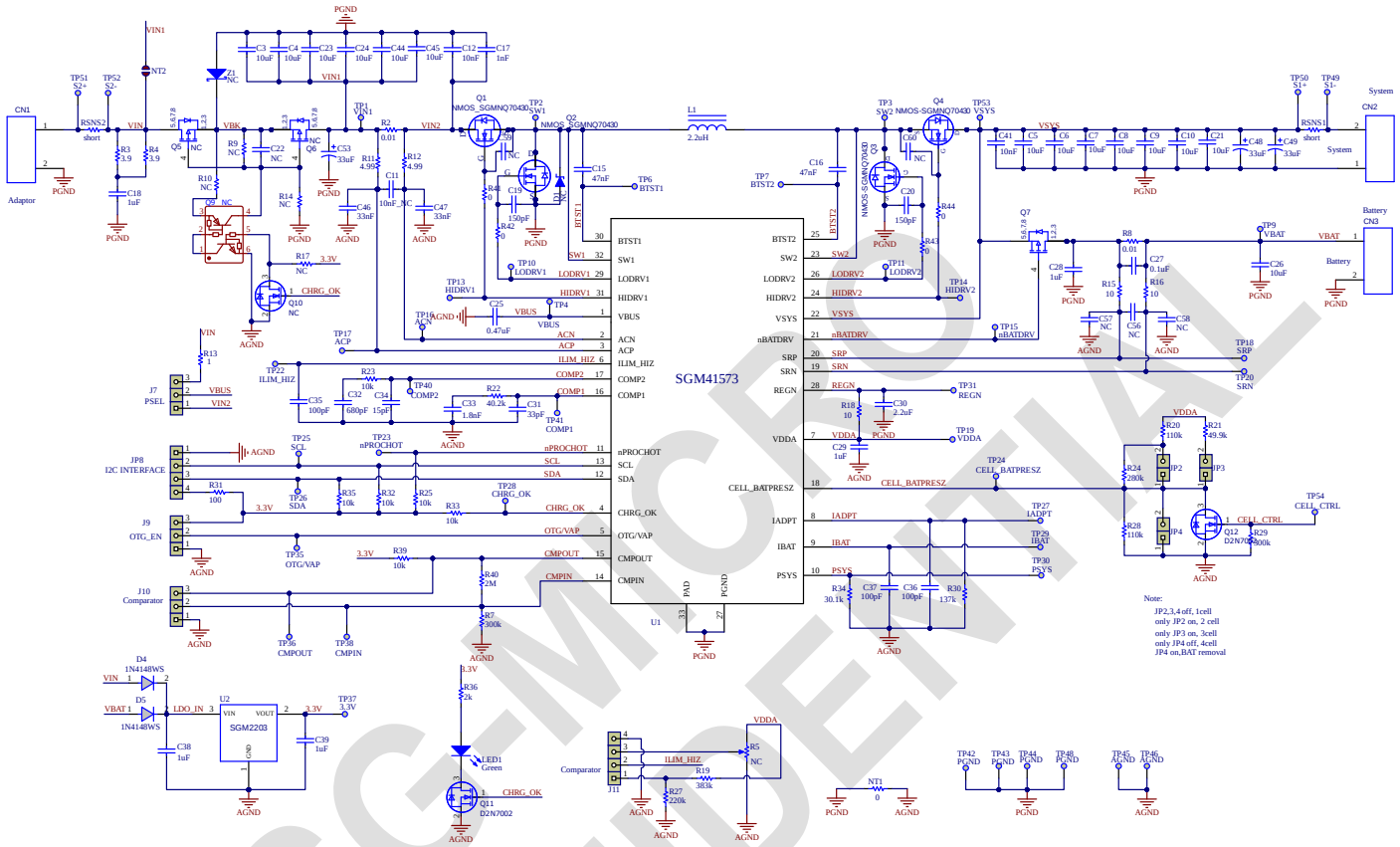
a. Change Adaptor output load can observe OTG mode load regulation and OTG output current limit.

b. Change battery emulator voltage can observe the OTG mode line regulation.

c. Other protections like OTG_OVP and OTG_UVP.

1.3 Demo Board Information

1.3.1 Schematic

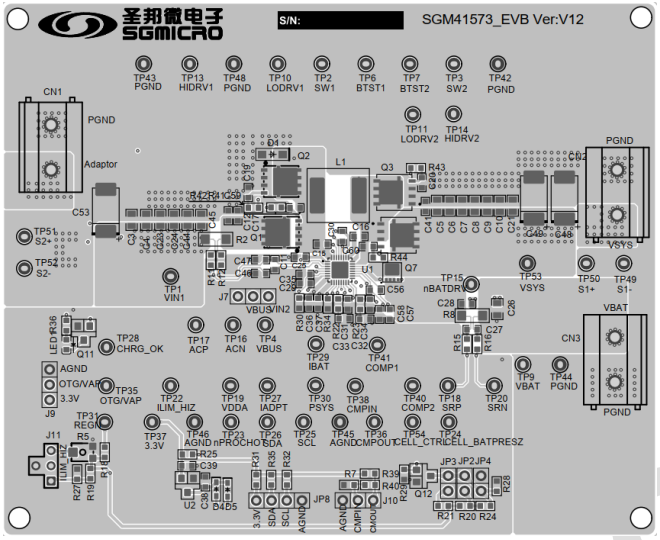


1.3.2 BOM List

Item	Quantity	Reference	Description
1	14	C3, C4, C5, C6, C7, C8, C9, C10, C21, C23, C24, C26, C44, C45	Ceramic capacitor, 10uF/25V, ±10%, X5R, 0805
2	0	C11, C22, C56, C57, C58, C59, C60	NC
3	2	C12, C41	Ceramic capacitor, 10nF/25V, ±10%, X7R, 0603
4	2	C15, C16	Ceramic capacitor, 47nF/25V, ±10%, X7R, 0603
5	1	C17	Ceramic capacitor, 1nF/100V, ±10%, X5R, 0603
6	5	C18, C28, C29, C38, C39	Ceramic capacitor, 1uF/25V, ±10%, X5R, 0603
7	2	C19, C20	Ceramic capacitor, 150pF/50V, ±10%, X7R, 0603
8	1	C27	Ceramic capacitor, 0.1uF/25V, ±10%, X7R, 0603
9	1	C25	Ceramic capacitor, 0.47uF/25V, ±10%, X5R, 0603
10	1	C30	Ceramic capacitor, 2.2uF/25V, ±10%, X5R, 0603
11	1	C31	Ceramic capacitor, 33pF/100V, ±5%, C0G, 0603
12	1	C32	Ceramic capacitor, 680pF/50V, ±5%, C0G, 0603
13	1	C33	Ceramic capacitor, 1.8nF/50V, ±10%, X7R, 0603
14	1	C34	Ceramic capacitor, 15pF/50V, ±5%, C0G, 0603
15	3	C35, C36, C37	Ceramic capacitor, 100pF/50V, ±5%, C0G, 0603
16	2	C46, C47	Ceramic capacitor, 33nF/25V, ±10%, X7R, 0603
17	3	C48, C49, C53	TA CAP, TPSE336K035R0100, 33uF, 35V, +/-10%, 0.1ohm, CASE-E_7343
18	3	CN1, CN2, CN3	Connector, C474954, KF128-7.5-2P
19	0	D1	NC
20	2	D4, D5	Diode, 1N4148WS, 0.1A, SOD323
21	3	JP2, JP3, JP4	Jumper for Cell setting: 1 Cell: JP2, JP3, JP4 all open 2 Cells: JP2 closed, JP3 and JP4 open 3 Cells: JP3 closed, JP2 and JP4 open 4 Cells: JP2 and JP3 closed, JP4 open BAT removal: JP4 closed
22	1	J7	Jumper: Left two connection Left two connection: V_{BUS} is connected to V_{IN} Right two connection: V_{BUS} is connected to V_{IN2}
23	1	JP8	Jumper: Communication Interface
24	1	J9	Jumper: Top two connection Top two connection: OTG/VAP is connected to 3.3V Bottom two connection: OTG/VAP is connected to GND
25	1	J10	Jumper: Open Bottom two connection: CMPIN is connected to GND
26	1	J11	Jumper: Bottom two connection Top two connection: ILIM_HIZ is connected to R5 Left two connection: ILIM_HIZ is connected to GND Bottom two connection: ILIM_HIZ is connected to resistor divider for setting external input current limit
27	1	L1	Inductor, 2.2uH, 74437356022, 8.5A, 0.0203ohm, Wurth

Item	Quantity	Reference	Description
28	1	LED1	LED, D-060306G1/SS2/G1,Green,0603
29	1	NT1	Short pad
30	1	NT2	Short pad
31	4	Q1, Q2, Q3, Q4	NMOSFET, SGMNQ70430, 30V, 46A, PDFN-5×6
32	0	Q5, Q6, Q9, Q10	NC
33	1	Q7	PMOSFET, CSD25402Q3A, -20V, -15A, VSONP-8
34	2	Q11, Q12	NMOSFET, 2N7002ET1G, 60 V, 0.26 A, SOT-23
35	2	R2, R8	Chip Resistor, PMR18EZPFU10L0, 10mΩ, 1W, 1%, 1206
36	2	R3, R4	Chip Resistor, 3.9Ω, 1/4W, 5%, 1206
37	0	R5	NC
38	2	R7, R29	Chip Resistor, 300kΩ, 1/10W, 5%, 0603
39	0	R9, R10, R14, R17	NC
40	3	R15, R16, R18	Chip Resistor, 10Ω, 1/10W, 1%, 0603
41	2	R11, R12	Chip Resistor, 4.99Ω, 1/10W, 1%, 0603
42	1	R13	Chip Resistor, 1Ω, 1/8W, 5%, 0805
43	6	R23, R25, R32, R33, R35, R39	Chip Resistor, 10k, 1/10W, 1%, 0603
44	1	R19	Chip Resistor,383kΩ, 1/10W, 1%, 0603
45	2	R20, R28	Chip Resistor, 110kΩ, 1/10W, 1%, 0603
46	1	R21	Chip Resistor, 49.9kΩ, 1/10W, 1%, 0603
47	1	R22	Chip Resistor, 40.2kΩ, 1/10W, 1%, 0603
48	1	R24	Chip Resistor, 280kΩ, 1/10W, 1%, 0603
49	1	R27	Chip Resistor, 220kΩ, 1/10W, 1%, 0603
50	1	R30	Chip Resistor, 137k, 1/10W, 1%, 0603
51	1	R31	Chip Resistor, 100Ω, 1/10W, 5%, 0603
52	1	R34	Chip Resistor, 30.1k, 1/10W, 1%, 0603
53	1	R36	Chip Resistor, 2kΩ, 1/10W, 5%, 0603
54	1	R40	Chip Resistor, 2MΩ, 1/10W, 5%, 0603
55	4	R41, R42, R43, R44	Chip Resistor, 0Ω, 1/10W, 1%, 0603
56	2	RSNS1, RSNS2	Short
57	1	U1	IC, SGM41573, NVDC Buck-Boost battery charge controller
58	1	U2	IC, SGM2203, 3.3V LDO, SOT23
59	0	Z1	NC

1.3.3 PCB Layout



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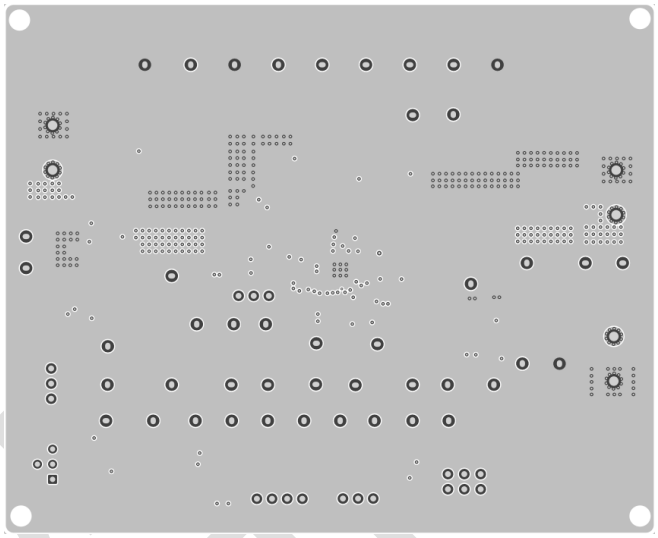
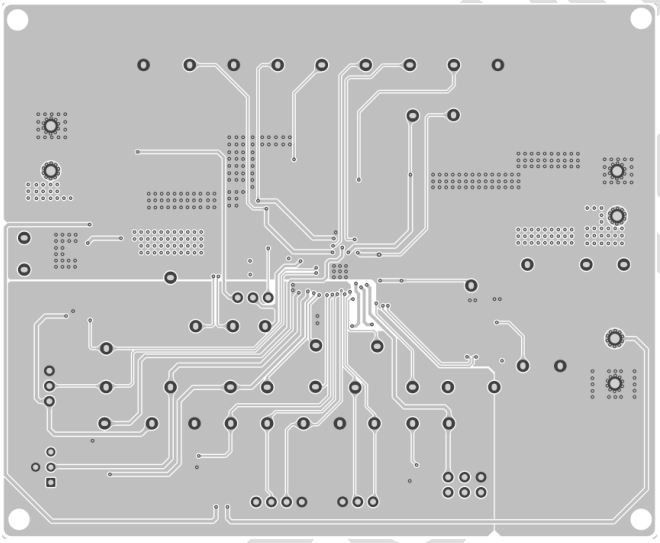
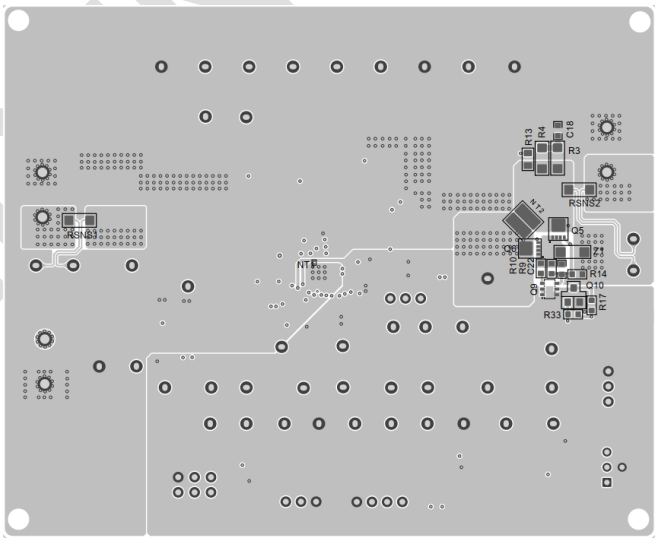


Mid-Layer1



Mid-Layer2



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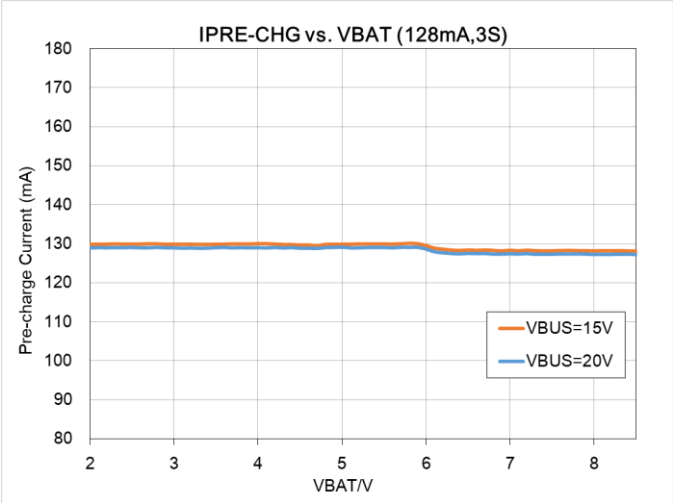
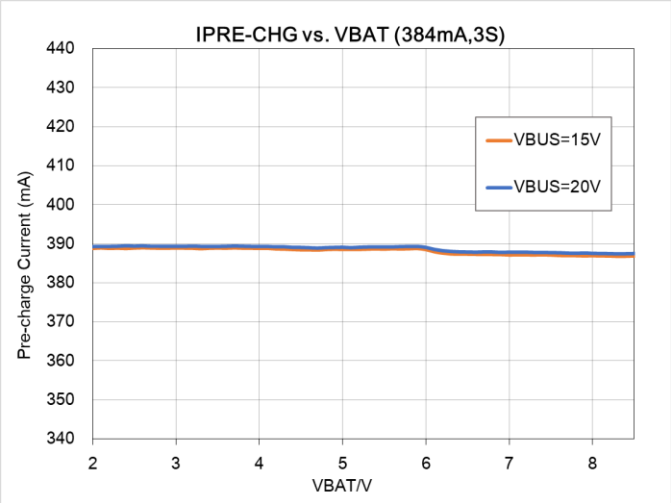
2. Demo Board Test Item

2.1 Pre-Charge Current

Test condition: 3S battery, V_{IN}=15V/20V, V_{SYSMIN} remain default setting (9.216V), I_{CHG_SET}=128mA/384mA, measure pre-charge current at different V_{BAT}.



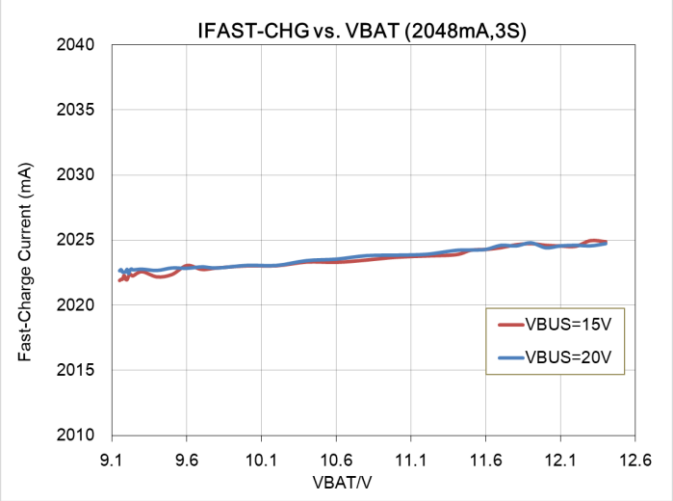
Pre-charge current curve with 3S battery, I_{CHG}=128mA



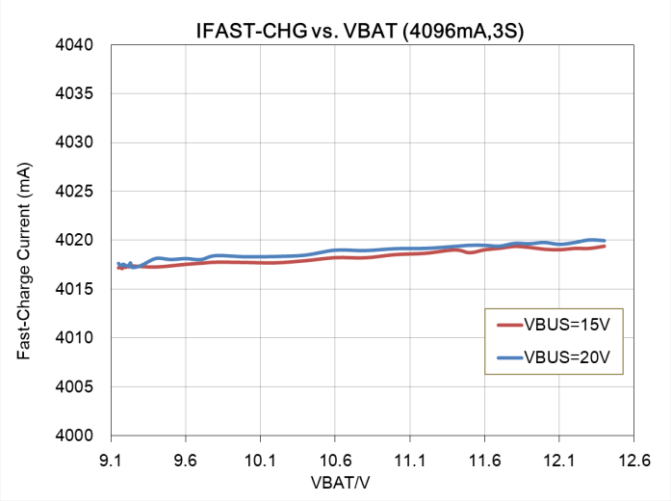
Pre-charge current curve with 3S battery, I_{CHG}=384mA

2.2 Fast Charge Current

Test condition: 3S battery, V_{IN}=15V/20V, V_{SYSMIN} remain default setting (9.216V), IIN_HOST set to 6350mA, disable EXTILIM, I_{CHG_SET}=2048mA/4096mA, measure fast charge current at different V_{BAT}.



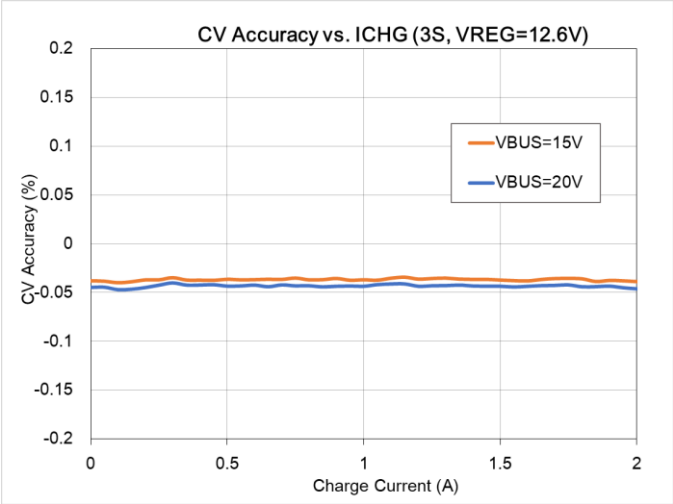
Fast charge current curve with 3S battery, I_{CHG}=2048mA



Fast charge current curve with 3S battery, I_{CHG}=4096mA

2.3 Constant Charge Voltage Accuracy

Test condition: 3S battery, V_{IN}=15V/20V, I_{CHG_SET}=2048mA, V_{REG}=12.6V, increase V_{BAT} close to V_{REG} and measure charge current at different V_{BAT}.



CV accuracy curve, 3S battery, V_{REG}=12.6V

2.4 IINDPM

Test condition: 3S battery, V_{IN}=15V/20V, V_{BAT}=11.4V, disable ILIM_HIZ pin, I_{CHG_SET}=8128mA, measure the differential voltage between ACP and ACN at different IIN_HOST setting.

V_{BUS}=15V			V_{BUS}=20V		
I_{DPM_SET}(A)	I_{INMAX}(A)	Accuracy	I_{DPM_SET}(A)	I_{INMAX}(A)	Accuracy
0.5	0.48	-3.60%	0.5	0.48	-3.40%
1	0.96	-3.70%	1	0.97	-3.20%
1.5	1.44	-3.87%	1.5	1.45	-3.20%
2	1.92	-3.95%	2	1.94	-3.25%
3	2.87	-4.27%	3	2.89	-3.53%
4	3.82	-4.58%	4	3.85	-3.88%

2.5 VINDPM

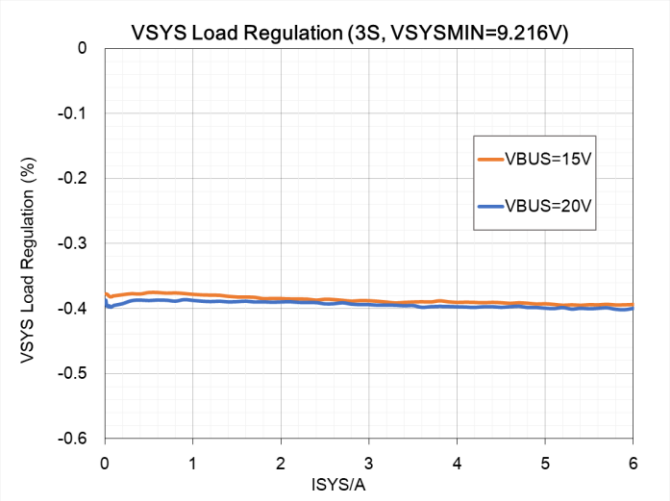
Test condition: 3S battery, V_{IN}=21V, set the current limit of the input power supply to 0.5A, V_{BAT}=11.4V, I_{CHG_SET}=2048mA, trigger VINDPM, and measure V_{BUS} at different Input Voltage Register setting.

VINDPM setting(V)	V_{INMIN}(V)	Accuracy
5.056	5.02	-0.71%
9.024	8.96	-0.71%
12.032	11.94	-0.76%
15.04	14.92	-0.80%
18.688	18.55	-0.74%
19.52	19.33	-0.97%

2.6 SYSMIN Load Regulation

Test condition: 3S battery, V_{IN}=15V/20V, V_{SYSMIN} remain default setting (3S-9.216V), V_{BAT}=2.9V, charge disable,

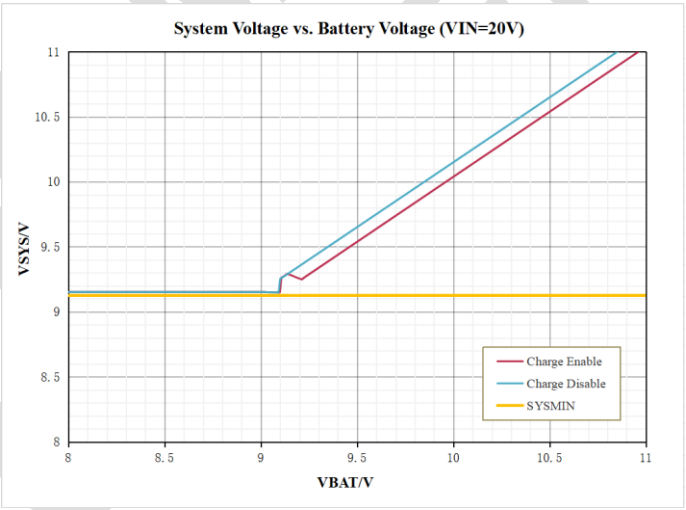
measure V_{SYS} at different system load current.



System Load Regulation, 3S battery, V_{SYSMIN}=9.216V

2.7 NVDC

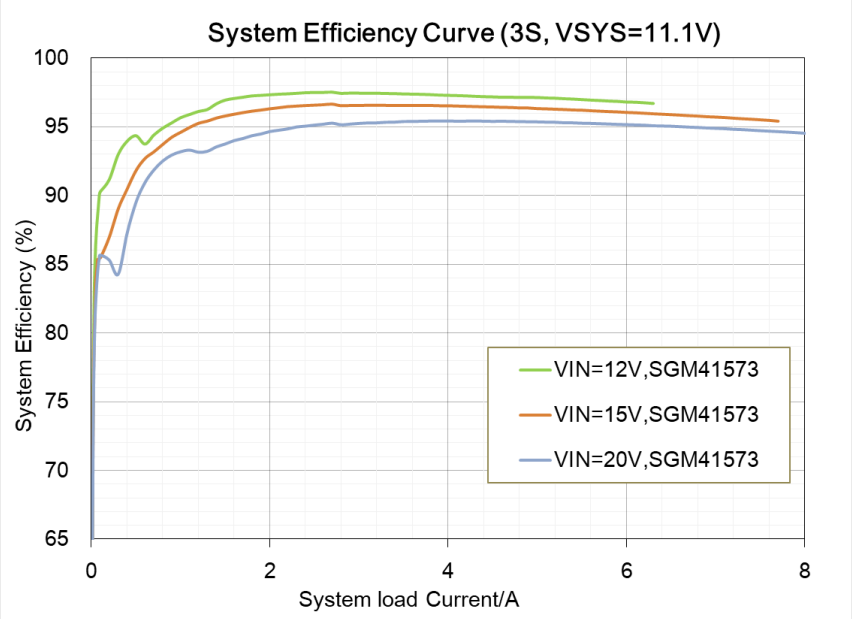
Test condition: 3S battery, V_{IN}=20V, V_{BAT}=8V~11V, V_{SYSMIN}=9.126V, charge disable/enable (I_{CHG}=2048mA), measure V_{SYS} at different V_{BAT}.



2.8 Efficiency

2.8.1 System Efficiency

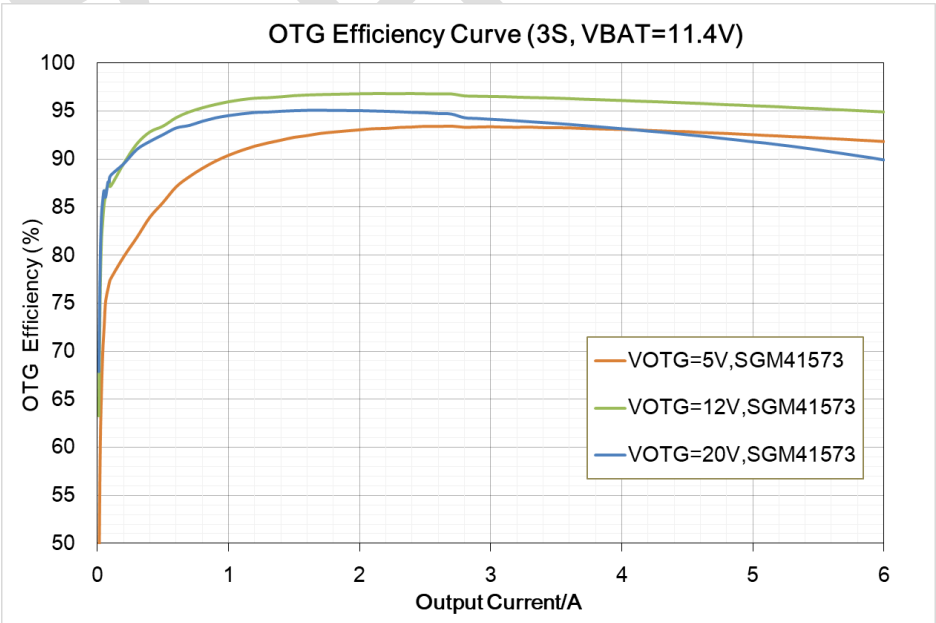
Test condition: 3S battery, V_{IN}=12V/15V/20V, charge disable, IDPM=6350mA, disable EXTILIM, set V_{BAT}=10.93V to hold V_{SYS}=11.11V, measure the system efficiency at different load current.



System Efficiency Curve, 3S battery, V_{SYS}=11.1V

2.8.2 OTG Efficiency

Test condition: 3S battery, V_{BAT}=11.4V, V_{OTG_SET}=5V/12V/20V, measure the OTG output efficiency at different load current.



OTG Efficiency Curve, 3S battery, V_{BAT}=11.4V

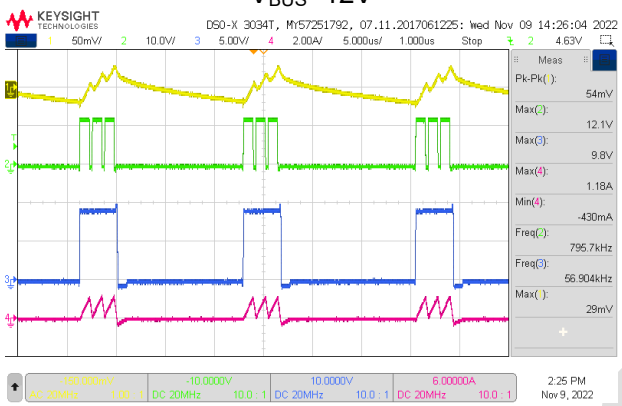
2.9 Steady State Operation

2.9.1 Charge Mode

2.9.1.1 Wakeup Mode

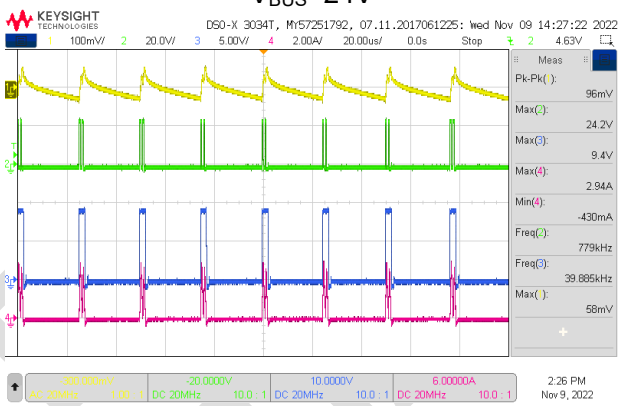
Test condition: 3 cells, V_{BUS}=12V/24V, V_{BAT}=9V, V_{SYSMIN}=9.216V, I_{CHG}=128mA, charge enable.

V_{BUS}=12V



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

V_{BUS}=24V

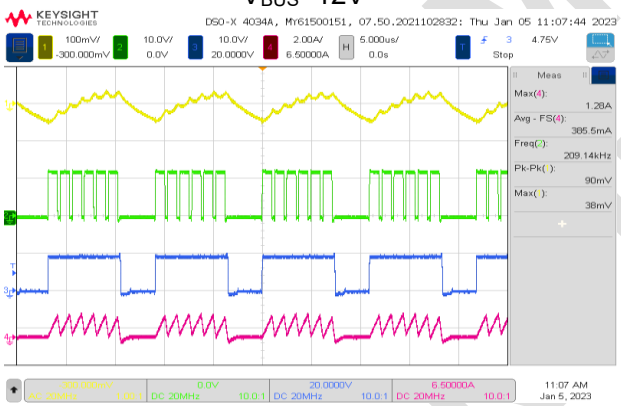


CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

2.9.1.2 Pre-charge Mode

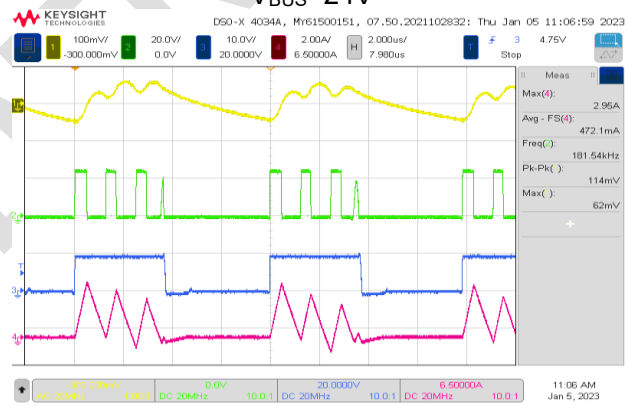
Test condition: 3 cells, V_{BUS}=12V/24V, V_{BAT}=9V, V_{SYSMIN}=9.216V, I_{CHG}=384mA, charge enable.

V_{BUS}=12V



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

V_{BUS}=24V

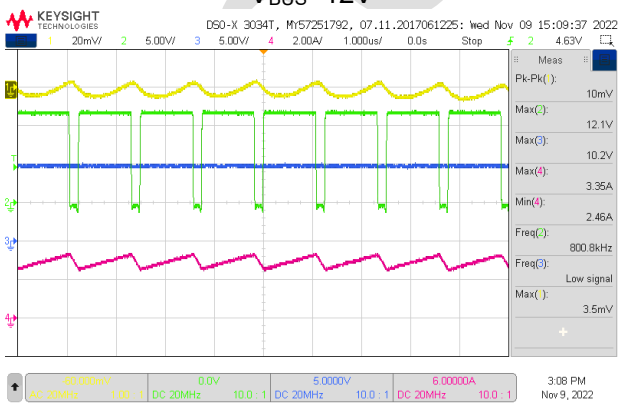


CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

2.9.1.3 CC-charge Mode

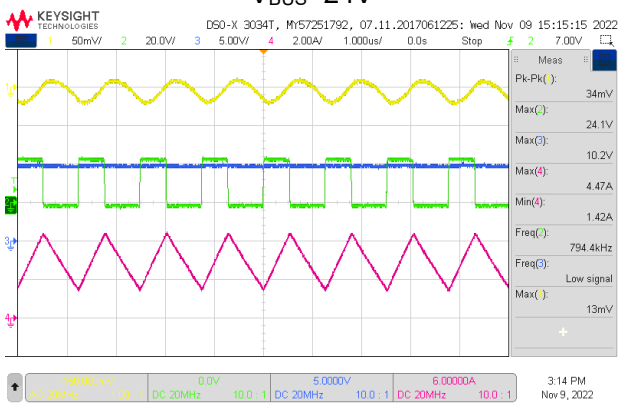
Test condition: 3 cells, V_{BUS}=12V/24V, V_{BAT}=10V, V_{SYSMIN}=9.216V, I_{CHG}=3A, charge enable.

V_{BUS}=12V



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

V_{BUS}=24V

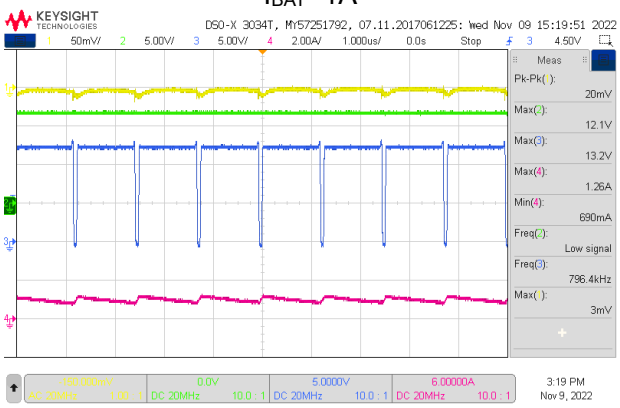


CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

2.9.1.4 CV-charge Mode

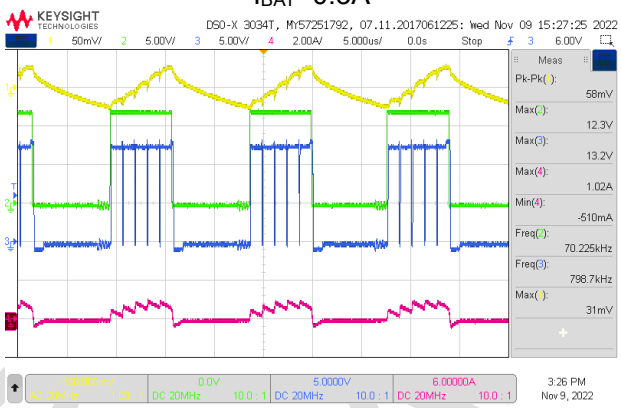
Test condition: 3 cells, V_{BUS}=12V, Charge voltage=12.6V, I_{CHG}=3A, charge enable.

I_{BAT}=1A



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

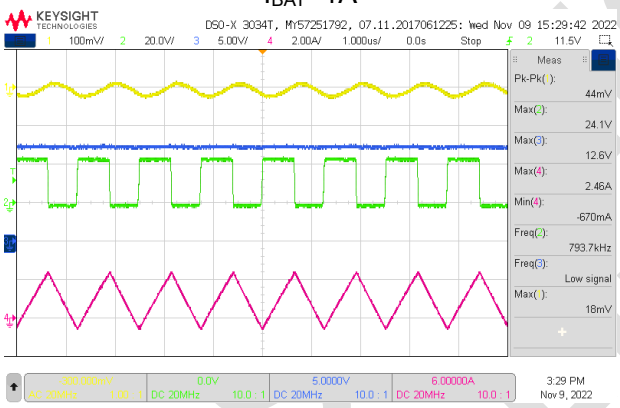
I_{BAT}=0.3A



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

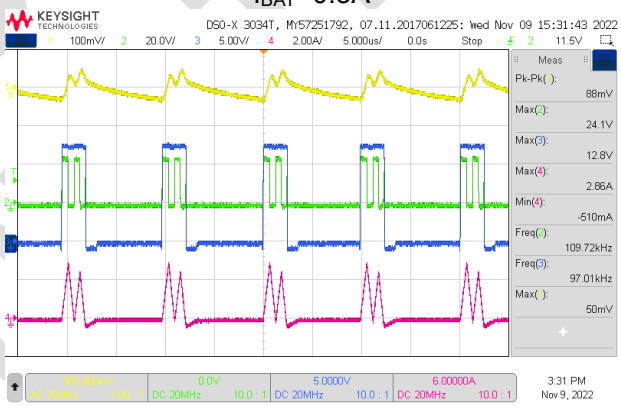
Test condition: 3 cells, V_{BUS}=24V, Charge voltage=12.6V, I_{CHG}=3A, charge enable.

I_{BAT}=1A



CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

I_{BAT}=0.3A

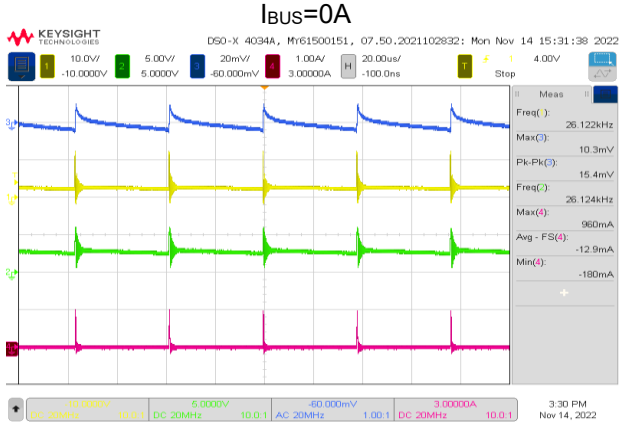


CH1-$V_{SYS/ac}$, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

2.9.2 OTG Mode

Test condition: 3 cells, V_{BAT}=12V, V_{BUS}=5V, OTG Current=6.35A, OTG mode, OOA enable.

I_{BUS}=0A

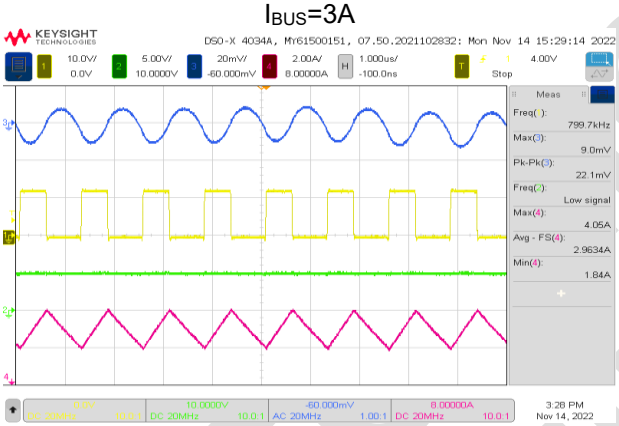


Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}/ac, Ch4-I_L

I_{BUS}=0.2A

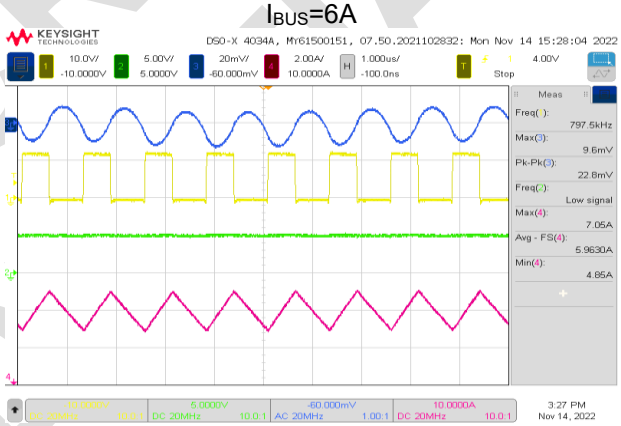
Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}/ac, Ch4-I_L

I_{BUS}=3A



Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}/ac, Ch4-I_L

I_{BUS}=6A

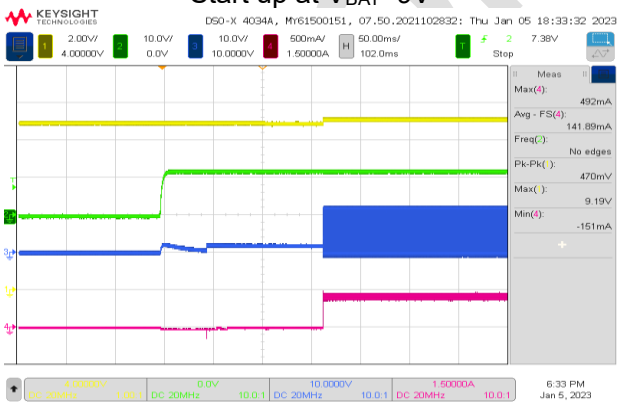


Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}/ac, Ch4-I_L

2.10 Charger Startup/Shutdown through VBUS

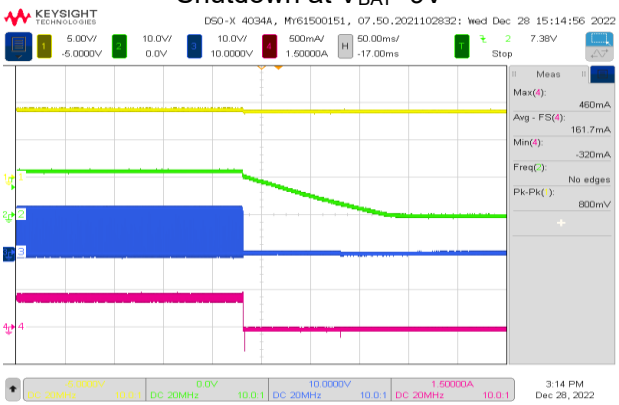
Test condition: 3 cells, V_{BUS}=12V, V_{BAT}=9V, V_{SYSMIN}=9.216V, set I_{CHG}=3A, plug in/out adaptor at different battery voltage.

Start up at V_{BAT}=9V



CH1-V_{SYS}, CH2-V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

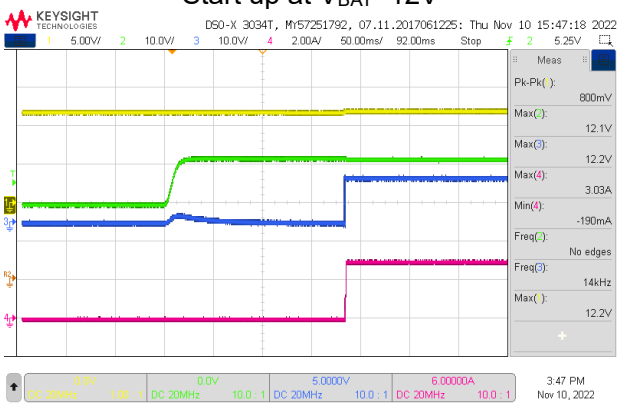
Shutdown at V_{BAT}=9V



CH1-V_{SYS}, CH2-V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

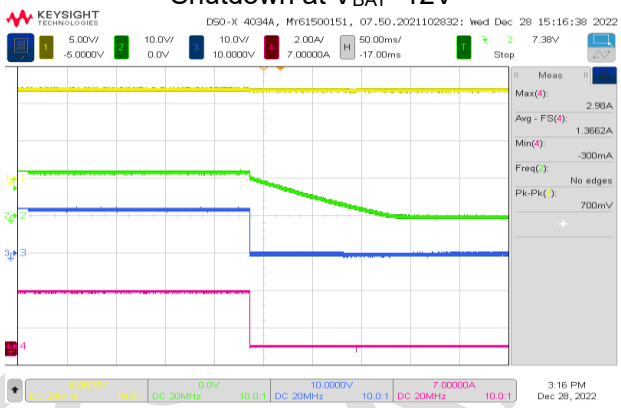
Test condition: 3 cells, V_{BUS}=12V, V_{BAT}=12V, V_{SYSMIN}=9.216V, set I_{CHG}=3A, plug in/out adaptor at different battery voltage.

Start up at V_{BAT}=12V



CH1-V_{SYS}, CH2-V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

Shutdown at V_{BAT}=12V

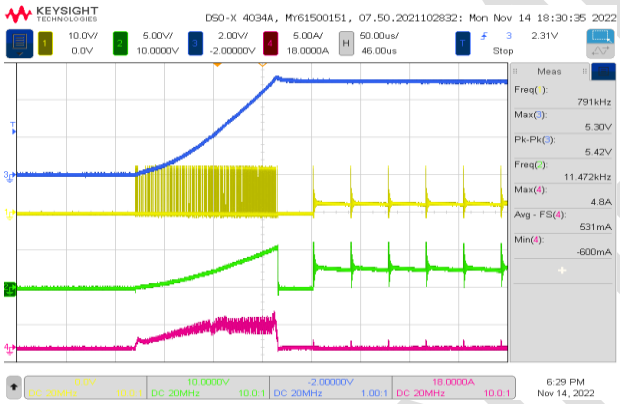


CH1-V_{SYS}, CH2-V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

2.11 Enter/Exit OTG

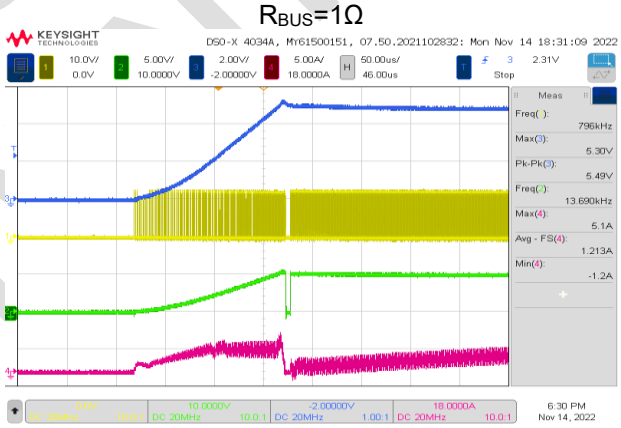
Test condition: V_{BAT}=12V, V_{BUS}=5V, OTG Current=6.35A, write EN OTG=1, OTG entry.

No Load



Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L

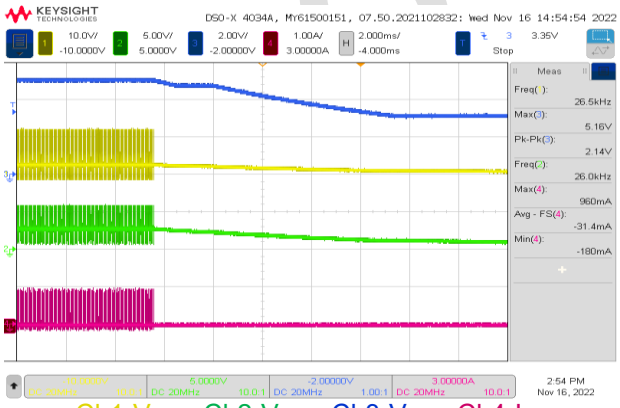
R_{BUS}=1Ω



Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L

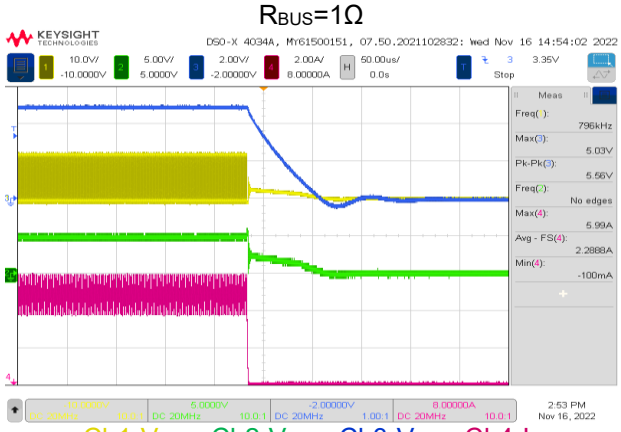
Test condition: V_{BAT}=12V, V_{BUS}=5V, OTG Current=6.35A, in OTG mode, write EN OTG=0, OTG exit.

No Load



Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L

R_{BUS}=1Ω

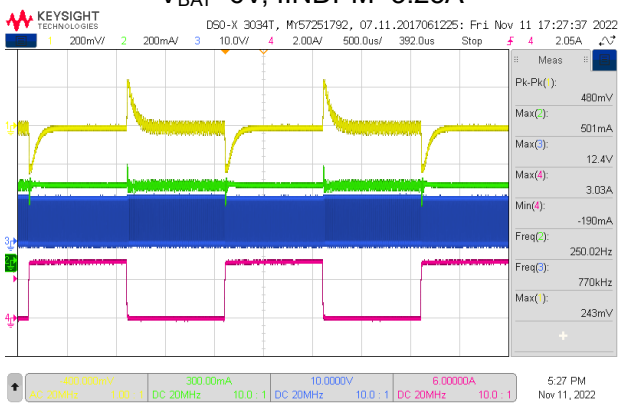


Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L

2.12 Dynamic System Load

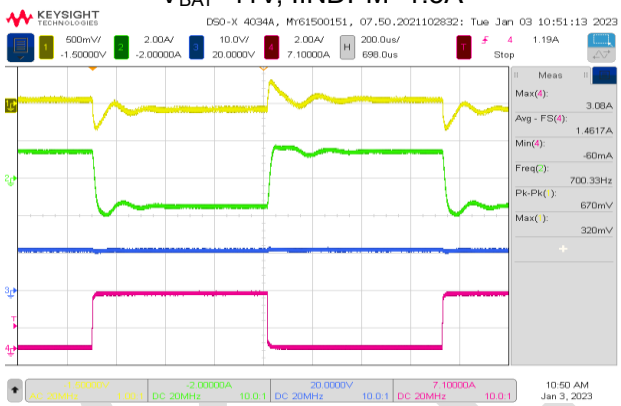
Test condition: 3 cells, V_{BUS}=12V, I_{CHG_SET}=3A, V_{SYSMIN}=9.216V, dynamic I_{SYS}=0A-3A-0A (slew rate =2.5A/us).

V_{BAT}=6V, IINDPM=3.25A



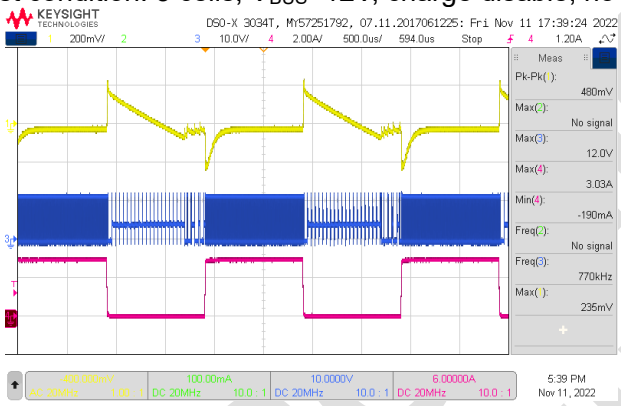
CH1-V_{SYS}/ac, CH2-I_{CHG}, CH3-V_{SW1}, CH4-I_{SYS}

V_{BAT}=11V, IINDPM=1.5A



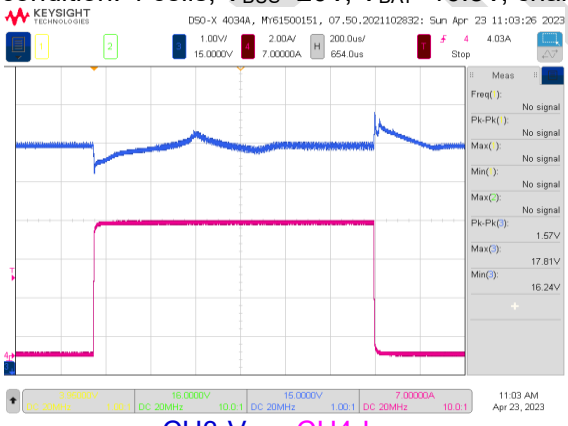
CH1-V_{SYS}/ac, CH2-I_{CHG}, CH3-V_{SW2}, CH4-I_{SYS}

Test condition: 3 cells, V_{BUS}=12V, charge disable, no battery, dynamic I_{SYS}=0A-3A-0A (slew rate =2.5A/us).



CH1-V_{SYS}/ac, CH3-V_{SW1}, CH4-I_{SYS}

Test condition: 4 cells, V_{BUS}=20V, V_{BAT}=16.8V, charge disable, dynamic I_{SYS}=0A-7A-0A (slew rate =2.5A/us).

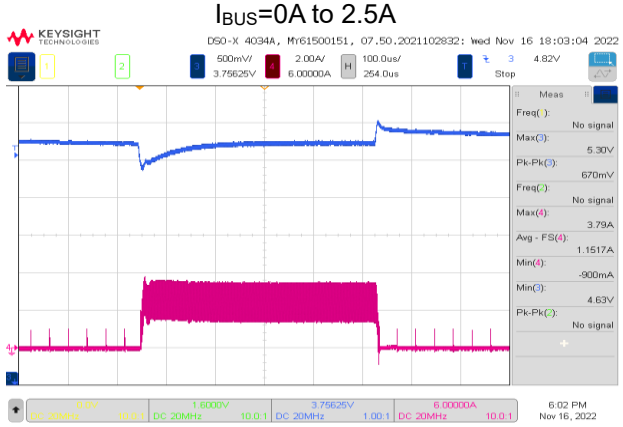


CH3-V_{SYS}, CH4-I_{SYS}

2.13 Dynamic BUS Load in OTG

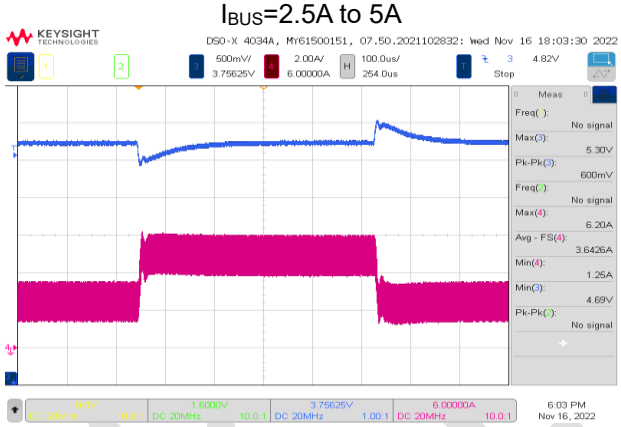
Test condition: V_{BAT}=12V, V_{BUS}=5V, OTG Current=6.35A, OTG mode, slew rate of I_{BUS} =2.5A/us.

I_{BUS}=0A to 2.5A



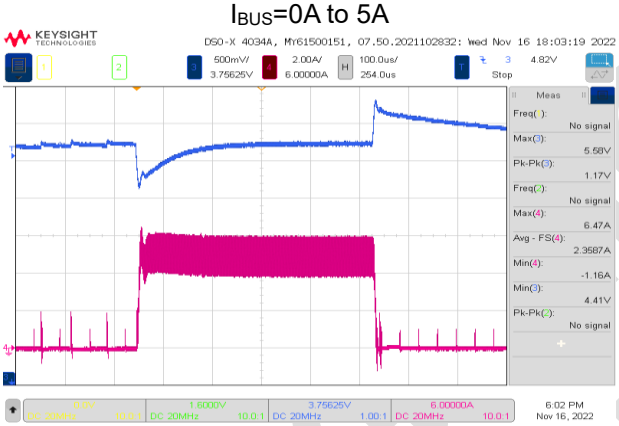
Ch3-V_{BUS}, Ch4-I_L

I_{BUS}=2.5A to 5A



Ch3-V_{BUS}, Ch4-I_L

I_{BUS}=0A to 5A

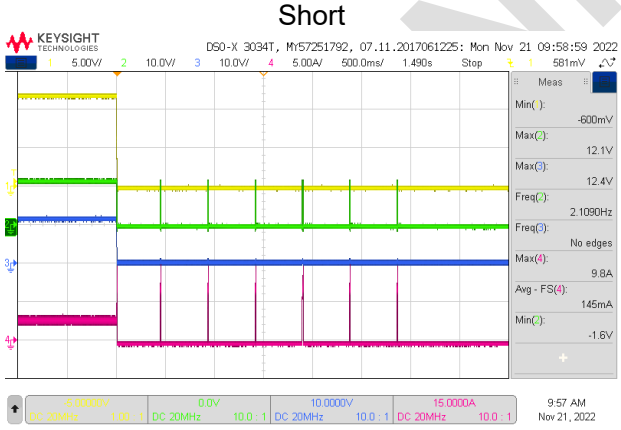


Ch3-V_{BUS}, Ch4-I_L

2.14 System SCP

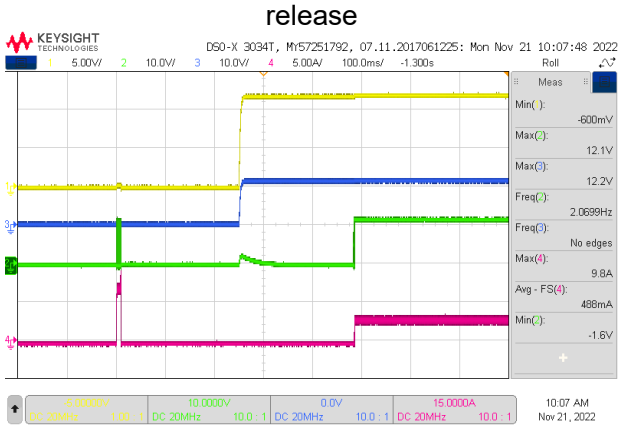
Test condition: 3 cells, V_{BUS}=12V, V_{BAT}=12V, I_{CHG}=3A, short system to GND, then release.

Short



CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

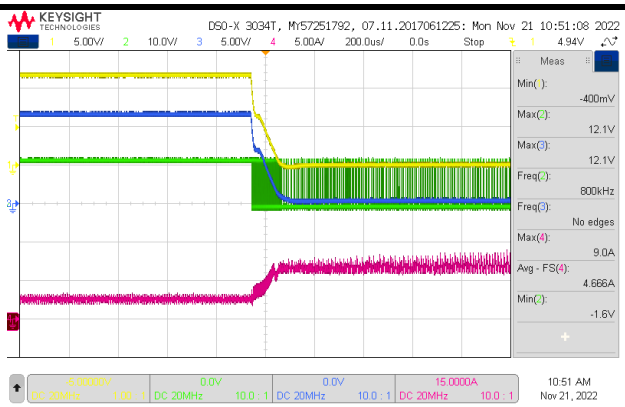
release



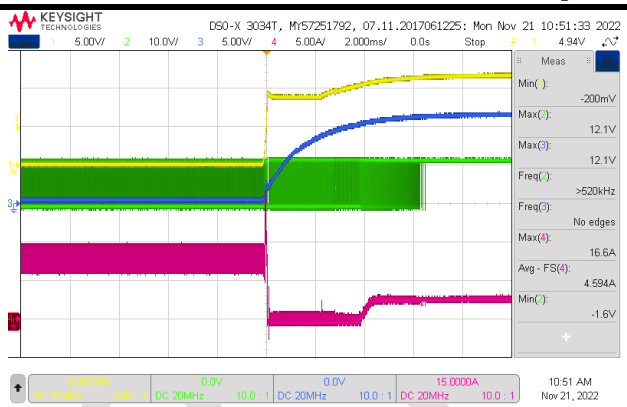
CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

Test condition: 3 cells, V_{BUS}=12V, V_{BAT}=12V, I_{CHG}=3A, disable hiccup, short system to GND, then release.

Short release



CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

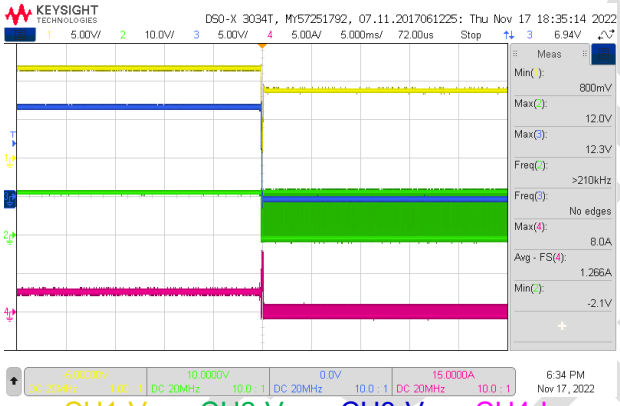


CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

2.15 Battery SCP

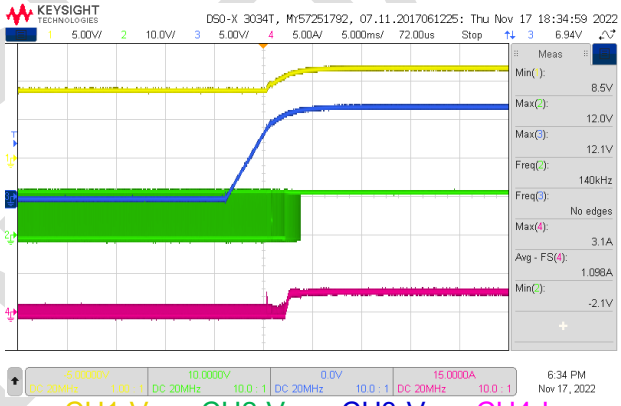
Test condition: V_{BUS}=12V, V_{BAT}=12V, I_{CHG}=3A, charge enable, short battery to GND, then release.

Short



CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

Release

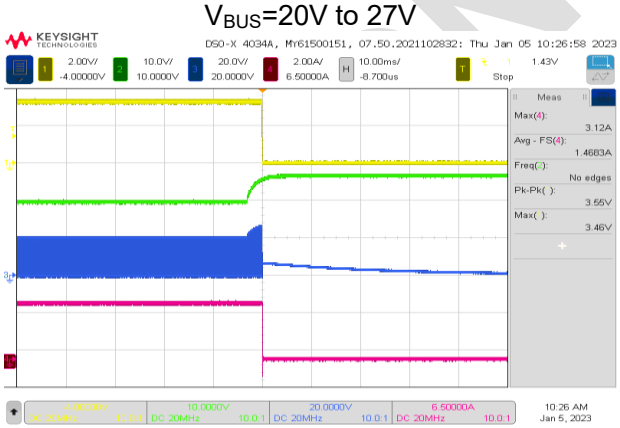


CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_L

2.16 VBUS OVP

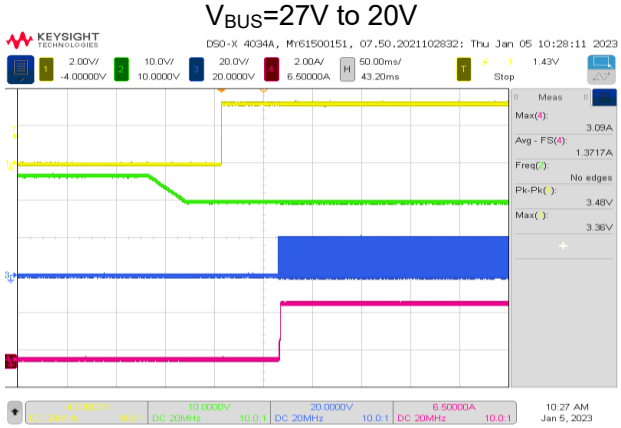
Test condition: 3 Cells, V_{BUS}=20V-27V, V_{BAT}=12V, charge enable, ICHG=3A.

V_{BUS}=20V to 27V



CH1-CHGOK, CH2- V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

V_{BUS}=27V to 20V

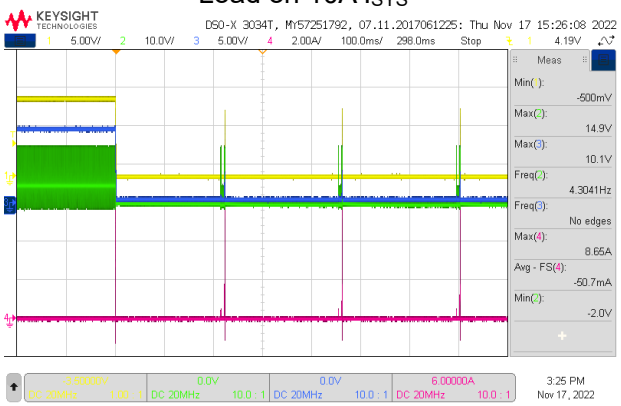


CH1-CHGOK, CH2- V_{BUS}, CH3-V_{SW1}, CH4-I_{CHG}

2.17 VBUS OC

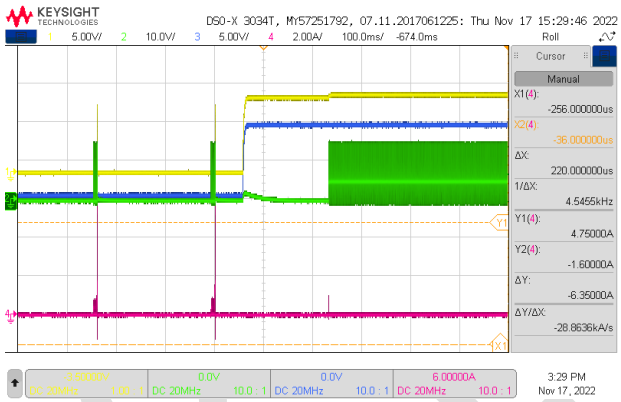
Test condition: 3 cells, V_{BUS}=15V, V_{BAT}=10V, charge disable, IDPM disable, enable ACOC, SET ILIM2=110%INHOST, ACOC=133%ILIM2, INHOST=3.25A.

Load on 10A I_{SYS}



CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_{BUS}

Remove SYS load

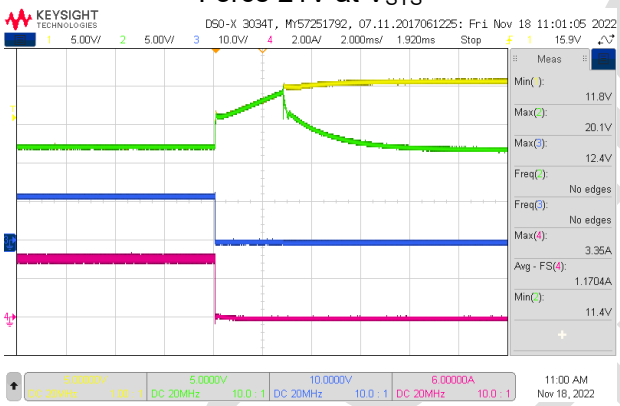


CH1-V_{SYS}, CH2-V_{SW1}, CH3-V_{BAT}, CH4-I_{BUS}

2.18 System OVP

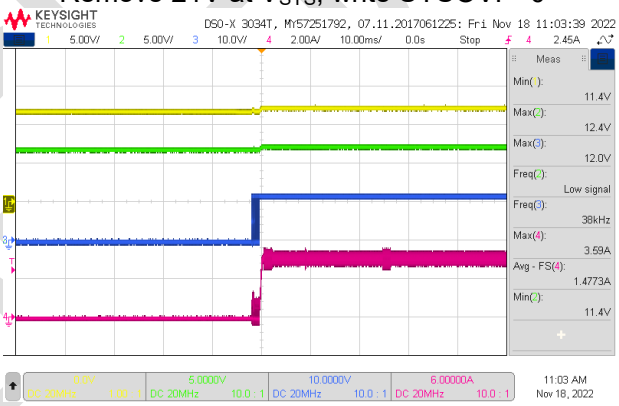
Test condition: 3 Cells, V_{BUS}=12V, V_{BAT}=12V, charge enable, I_{CHG}=3A, force a 21V external power supply on system.

Force 21V at V_{SYS}



CH1-V_{SYS}, CH2-V_{BAT}, CH3-V_{SW1}, CH4-I_L

Remove 21V at V_{SYS}, write SYSOVP=0

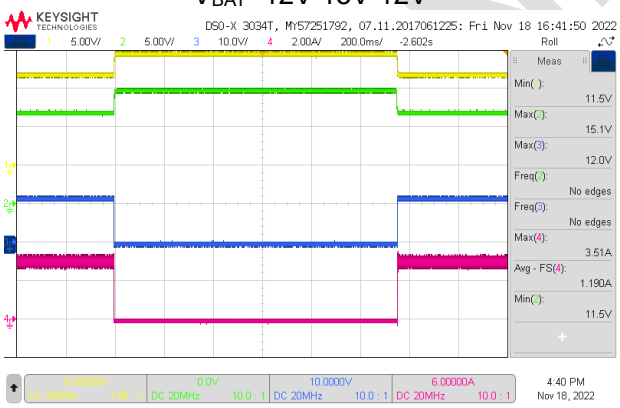


CH1-V_{SYS}, CH2-V_{BAT}, CH3- V_{SW1}, CH4-I_L

2.19 VBAT OVP

Test condition: 3 Cells, V_{BUS}=12V, V_{SYSMIN}=9.216V, V_{BAT}=12V-15V, charge enable, ICHG=3A.

V_{BAT}=12V-15V-12V

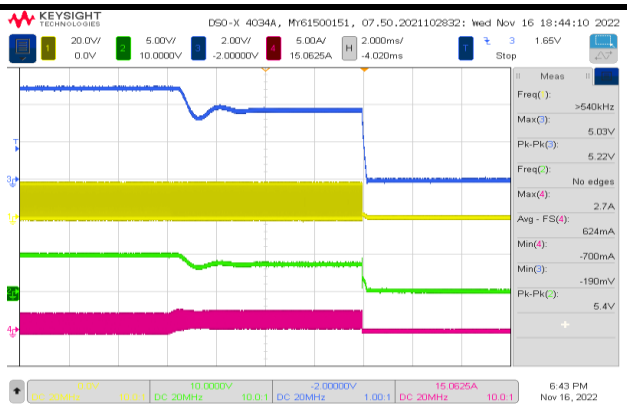


CH1-V_{SYS}, CH2-V_{BAT}, CH3-V_{SW1}, CH4-I_L

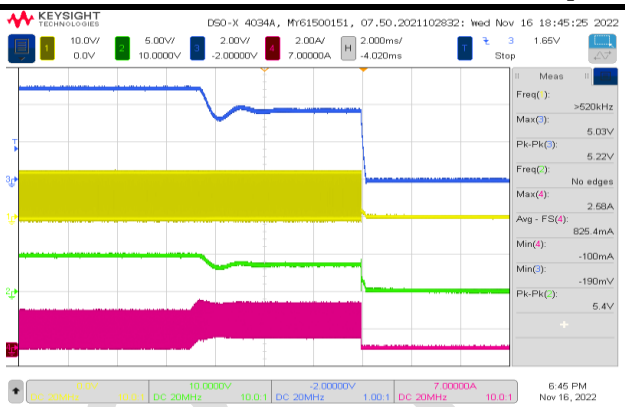
2.20 BUS UVP in OTG

Test condition: V_{BAT}=18V/12V, V_{BUS}=5V, OTG Current=1.5A, in OTG mode, R_{BUS}=5Ω to 2.5Ω.

V_{BAT}=18V V_{BAT}=12V

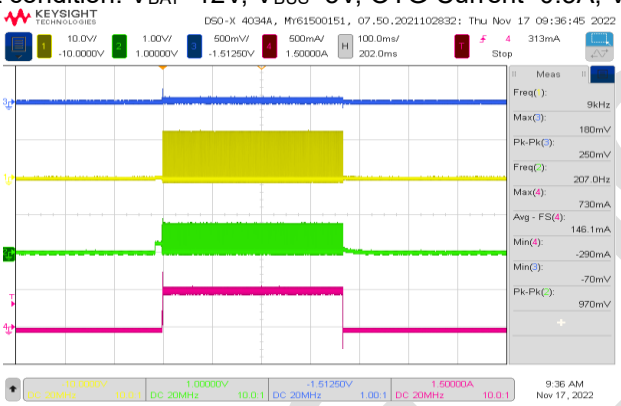


Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L



Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_L

Test condition: V_{BAT}=12V, V_{BUS}=5V, OTG Current=0.5A, V_{BUS} short, write EN OTG=1.

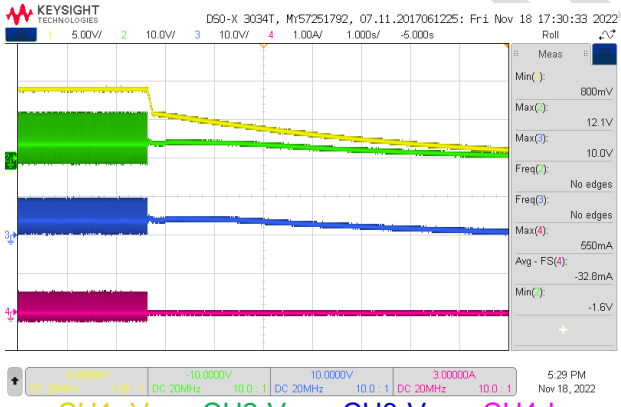


Ch1-V_{SW2}, Ch2-V_{SW1}, Ch3-V_{BUS}, Ch4-I_{BUS}

2.21 Thermal Shutdown

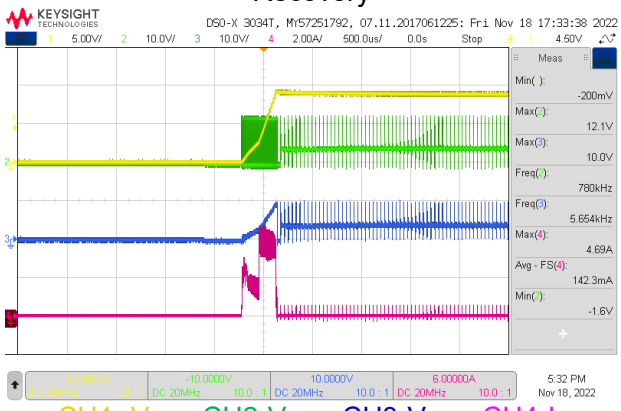
Test condition: V_{BUS}=12V, no BAT, charge disable, V_{SYSMIN}=9.216V, heat the part by the hot gun, I_{SYS}=0A

Thermal shutdown



CH1- V_{SYS}, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

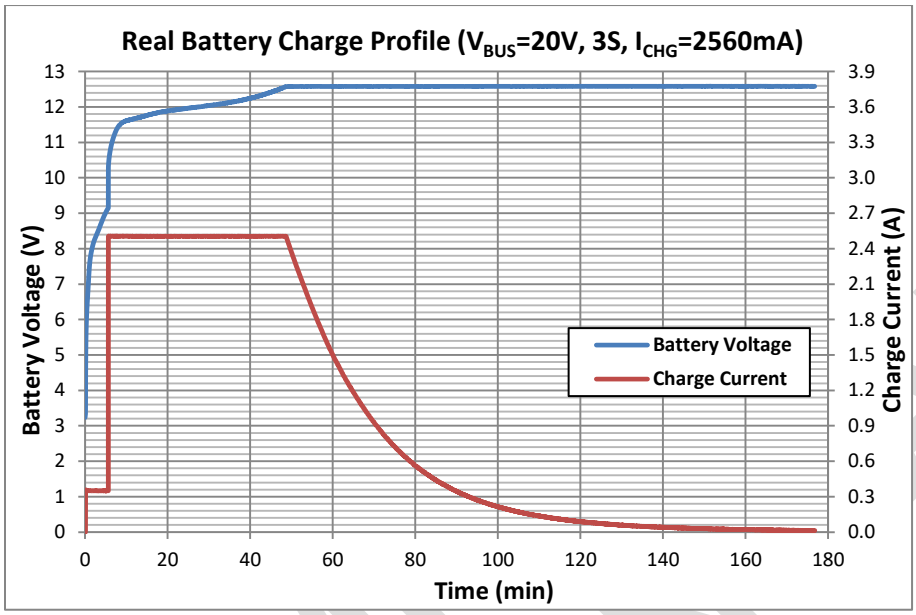
Recovery



CH1- V_{SYS}, CH2-V_{SW1}, CH3-V_{SW2}, CH4-I_L

2.22 Real Battery Charge Profile

Test condition: 3S battery, V_{IN}=20V, IIN_HOST set to 6350mA, disable EXTILIM, I_{CHG}=2560mA, do real battery charge test.



Real battery charge profile with 3S battery and V_{IN}=20V, I_{CHG}=2560mA

2.23 Component Temperature Rise

Test Condition：4S battery, V_{IN}=20V, V_{SYSMIN}=6.4V，I_{INDPM}=6350mA，disable EXTILIM, VBAT=9V，record the temperature of each device.

Ambient Temperature：T_A=27.8℃

I_{CHG}	SGM41570	Q1	Q2	Q3	Q4	BATFET	L
0	30.7	28.6	28.5	28.2	28.4	28.3	28.5
2496mA	40.0	47.5	42.8	38.1	37.8	36.5	40.0
4992mA	51.3	67.3	59.5	51.0	52.3	50.2	63.1

Test Condition： 4S battery, V_{IN}=20V, V_{SYSMIN}=6.4V，I_{INDPM}=6350mA，disable EXTILIM, V_{BAT}=17.6V，record the temperature of each device.

Ambient Temperature：T_A=27.8℃

I_{CHG}	SGM41570	Q1	Q2	Q3	Q4	BATFET	L
0	30.5	29.2	28.9	28.8	28.8	28.8	28.9
2496mA	45.1	51.0	42.7	39.2	38.3	38.5	42.5
4992mA	67.5	81.1	67.5	69.5	67.4	60.0	71.4