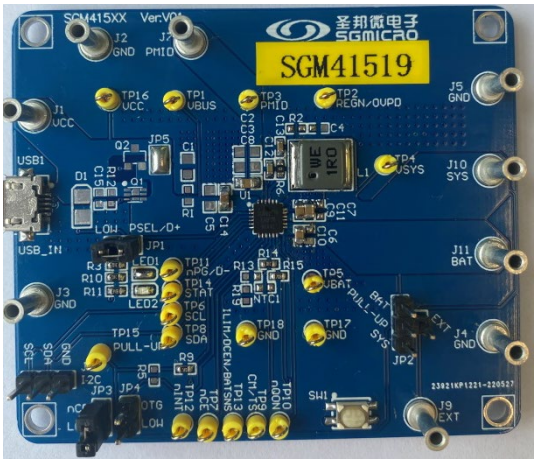
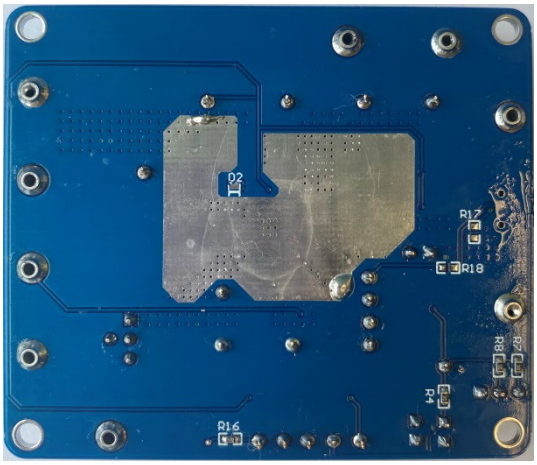
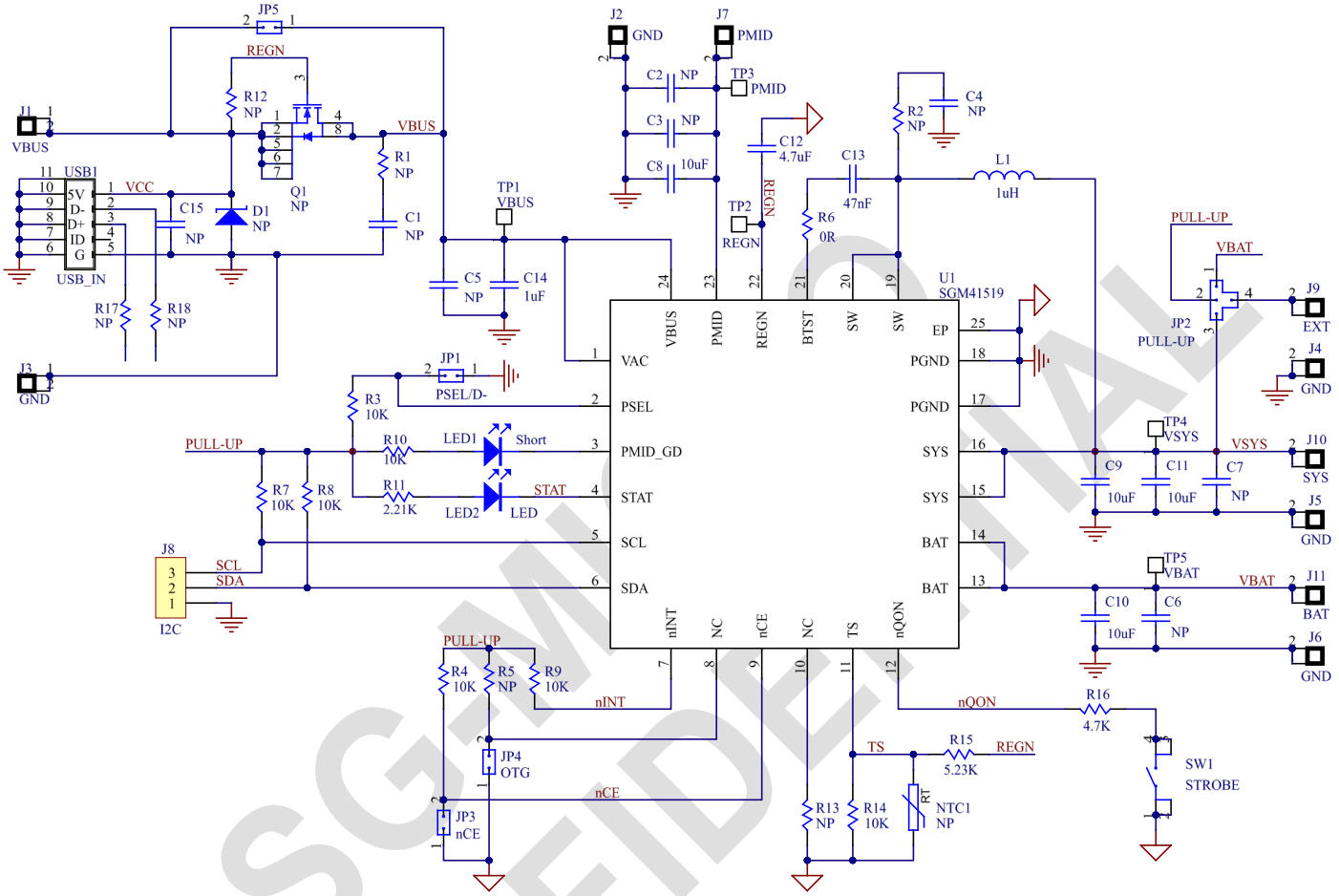
# SGM41519 Demo Board Test Report



## Table of Contents

## 1 Schematic and BOM List



| Item | Designator | QTY | Description | Manufactory |
|---|---|---|---|---|
| 1 | C1,C2,C3,C4,C5,C6,C7,C15 | 0 | NP | |
| 2 | C8 | 1 | 10uF,25V,X5R,0805 | |
| 3 | C9,C10,C11 | 3 | 10uF,10V,X5R,0805 | |
| 4 | C12 | 1 | 4.7uF,10V,X5R,0603 | |
| 5 | C13 | 1 | 47nF,25V,X5R,0603 | |
| 6 | C14 | 1 | 1uF,25V,X5R,0805 | |
| 7 | D1 | 0 | NP | |
| 8 | JP5 | 1 | Short | |
| 9 | L1 | 1 | 1uH, $I_{SAT}$=27.5A, $I_{RMS}$=12A, DCR=5.5mΩ, Size 6030，74439344010 | Wurth |
| 10 | LED1 | 1 | Short | |
| 11 | LED2 | 1 | LED, 0603, Green | |
| 12 | Q1 | 0 | NP | |
| 13 | R1,R2, R5,R12,R13,NTC1 | 0 | NP | |
| 14 | R3,R10,R4,R7,R8,R9 | 6 | 10KΩ, ±1%, SMD res.,0603 | |
| 15 | R6 | 1 | 0Ω, ±1%, SMD res.,0603 | |
| 16 | R17,R18 | 0 | NP | |
| 17 | R11 | 1 | 2.21KΩ, ±1%, SMD res.,0603 | |
| 18 | R14 | 1 | 10KΩ, ±1%, SMD res.,0603 | |
| 19 | R15 | 1 | 5.23KΩ, ±1%, SMD res.,0603 | |
| 20 | R16 | 1 | 4.7KΩ, ±5%, SMD res.,0603 | |
| 21 | SW1 | 1 | Tact Switch, SKRPACE010, SMD | |
| 22 | U1 | 1 | Charger IC, TQFN-4*4-24L, SGM41519 | SG-Micro |
| Conclusion: Total 24 components | | | | |

# 2 Test item

## 2.1 Trickle charge current

Test condition: $V_{BUS}$=5V~12V, $V_{BAT}$=0.1V~2.2V, charge enable, measure the charge current at different $V_{BAT}$.

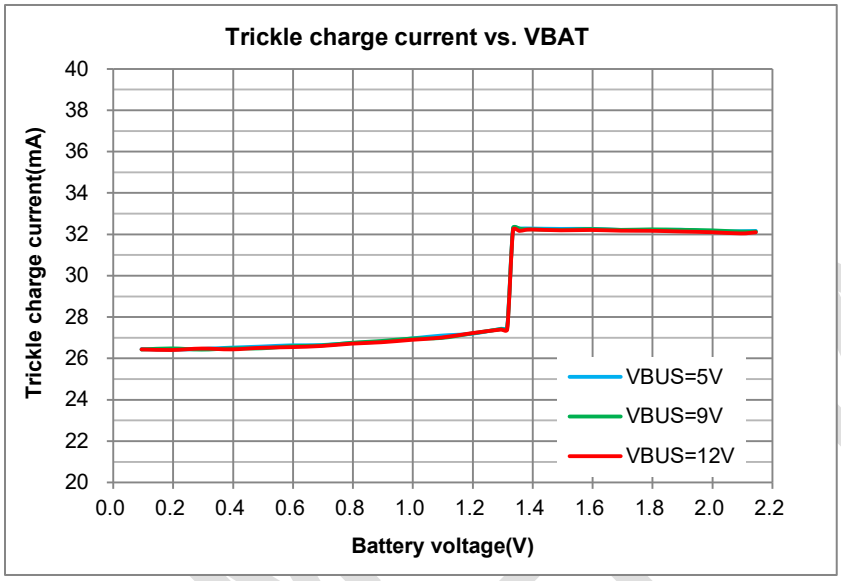



**Chart1** Trickle charge current vs. VBAT

## 2.2 Pre-charge current

Test condition: $V_{BUS}$=5V~12V, $V_{BAT}$=2.2V~3.15V, $I_{PRECHG\_SET}$=40mA, charge enable, measure the charge current at different $V_{BAT}$.

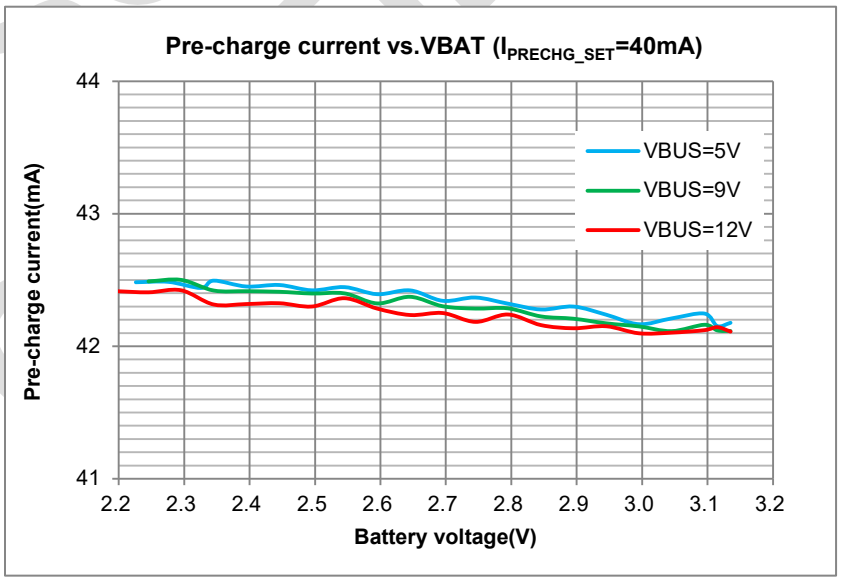



**Chart2** 40mA pre-charge current

### 2.3 Fast charge current

Test condition: $V_{BUS}$=5V~12V, $V_{BAT}$=3.2V~4.6V, $V_{BAT\_REG}$=4.624V, $I_{CHG\_SET}$=330mA, charge enable, measure the charge current at different $V_{BAT}$.

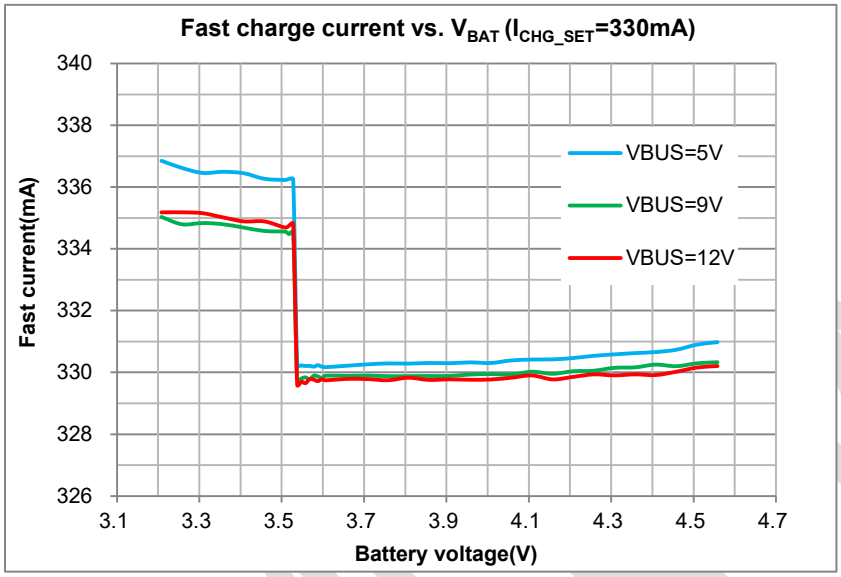



**Chart3** 330mA fast charge current

### 2.4 CV Accuracy

Test condition: $V_{BUS}$=5V/12V, $V_{BAT\_REG}$=3.856V/4.208V/4.352V/4.440V/4.624V, $I_{INDPM}$=3200mA, $I_{CHG}$=3000mA, $I_{TERM}$=5mA, charge enable, increase $V_{BAT}$ to enter CV charge, measure $V_{BAT}$ at different charge current.

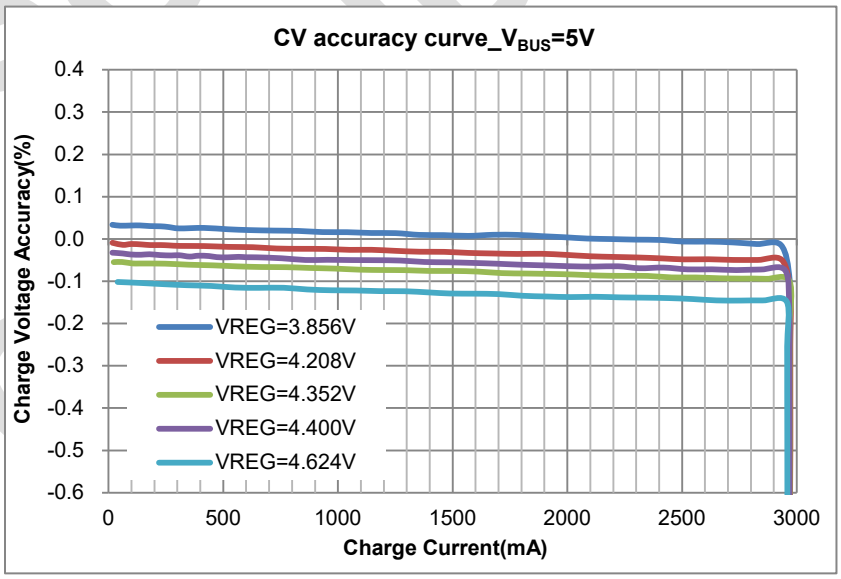



**Chart4** Charging voltage accuracy at VBUS=5V

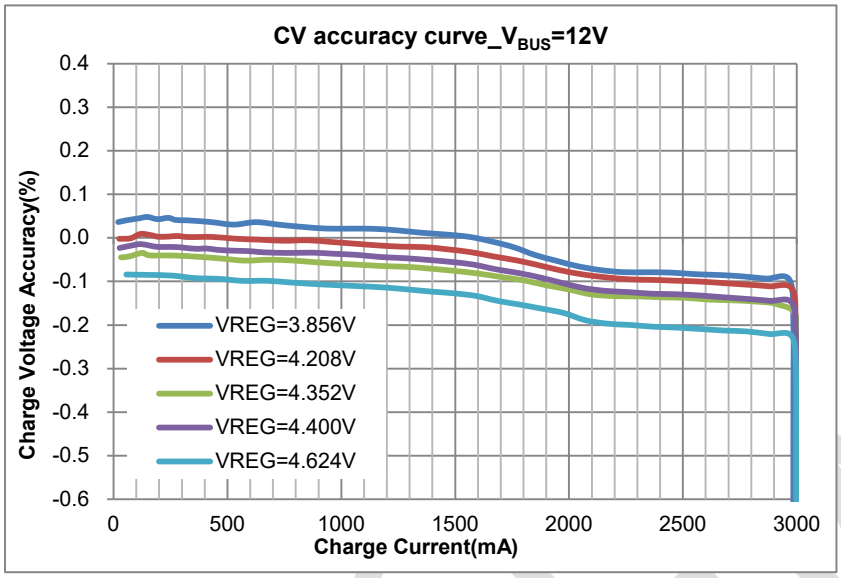



**Chart5** Charging voltage accuracy at VBUS=12V

## 2.5 Termination current Accuracy

Test condition: $V_{BUS}$=5V/9V/12V, $V_{BAT\_REG}$=4.208V, $I_{CHG\_SET}$=1020mA, $I_{TERM\_SET}$=5mA~240mA, charge enable, adjust $V_{BAT}$ to check termination current.

| $V_{BUS}$=5V | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{TERM\_SET}$(mA) | 5 | 10 | 15 | 20 | 30 | 40 | 50 | 60 | 80 | 100 | 120 | 140 | 160 | 180 | 200 | 240 |
| $I_{TERM}$(mA) | 9.9 | 13.9 | 19.5 | 24.3 | 35.3 | 44.9 | 55.2 | 65.6 | 84.7 | 104.6 | 124.6 | 144.3 | 164.2 | 184.2 | 204.2 | 244.0 |
| Error(mA) | 4.9 | 3.9 | 4.5 | 4.3 | 5.3 | 4.9 | 5.2 | 5.6 | 4.7 | 4.6 | 4.6 | 4.3 | 4.2 | 4.2 | 4.2 | 4.0 |
| $V_{BUS}$=9V | | | | | | | | | | | | | | | | |
| $I_{TERM\_SET}$(mA) | 5 | 10 | 15 | 20 | 30 | 40 | 50 | 60 | 80 | 100 | 120 | 140 | 160 | 180 | 200 | 240 |
| $I_{TERM}$(mA) | 8.4 | 14.0 | 18.7 | 24.2 | 34.8 | 44.4 | 54.1 | 64.5 | 84.1 | 104.7 | 124.6 | 144.6 | 163.5 | 184.2 | 204.1 | 242.9 |
| Error(mA) | 3.4 | 4.0 | 3.7 | 4.2 | 4.8 | 4.4 | 4.1 | 4.5 | 4.1 | 4.7 | 4.6 | 4.6 | 3.5 | 4.2 | 4.1 | 2.9 |
| $V_{BUS}$=12V | | | | | | | | | | | | | | | | |
| $I_{TERM\_SET}$(mA) | 5 | 10 | 15 | 20 | 30 | 40 | 50 | 60 | 80 | 100 | 120 | 140 | 160 | 180 | 200 | 240 |
| $I_{TERM}$(mA) | 8.4 | 13.3 | 18.7 | 23.8 | 34.0 | 44.4 | 54.0 | 64.4 | 83.6 | 103.6 | 124.5 | 144.1 | 163.8 | 183.8 | 203.6 | 243.3 |
| Error(mA) | 3.4 | 3.3 | 3.7 | 3.8 | 4.0 | 4.4 | 4.0 | 4.4 | 3.6 | 3.6 | 4.5 | 4.1 | 3.8 | 3.8 | 3.6 | 3.3 |

### 2.6 IINDPM

Test condition: $V_{BUS}$=5V/9V/12V, $V_{BAT}$=3.8V, $I_{CHG\_SET}$=3000mA, charge enable, $C_{PMID}$=2*10μF, increase $I_{SYS}$ to check $I_{INMAX}$ at different IINDPM bits setting.

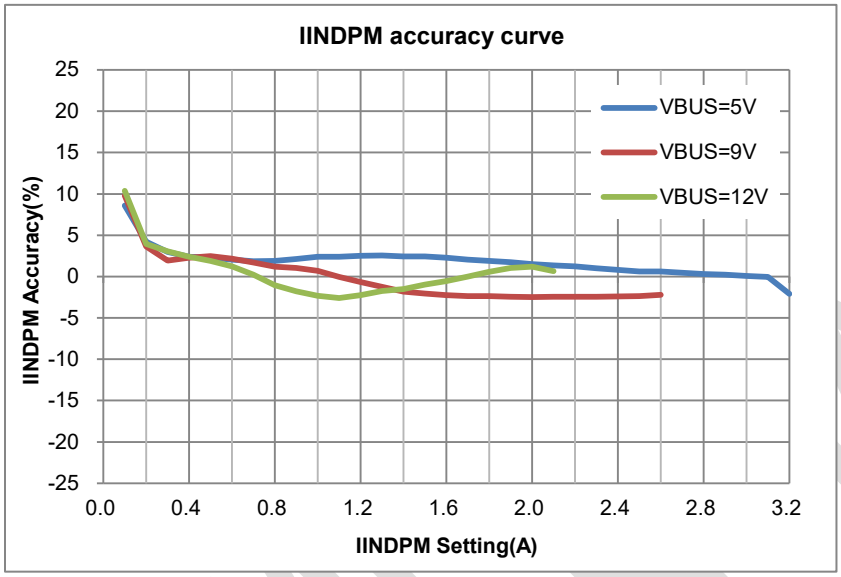



**Chart6** IINDPM accuracy at VBUS=5V/9V/12V

### 2.7 VINDPM

Test condition: $V_{BUS}$=13V/0.5A, VBUS_OV set to 14V, $V_{BAT}$=3.8V, $V_{SYS\_MIN}$=3.5V, $I_{CHG\_SET}$=3000mA, $I_{INDPM\_SET}$=3.2A, charge enable, measure $V_{BUS}$ at different VINDPM bits (VINDPM_OS, VINDPM register) setting.

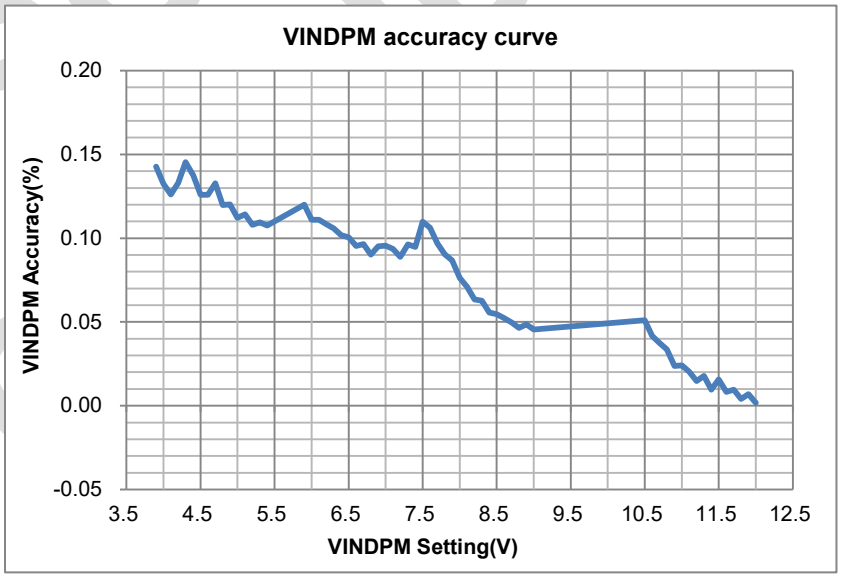



**Chart7** VINDPM accuracy

## 2.8 Charging efficiency

Test condition: $V_{BUS}$=5V/9V/12V, $V_{BAT}$=3.8V, $I_{SYS}$=0A, charge enable, measure the charge efficiency.

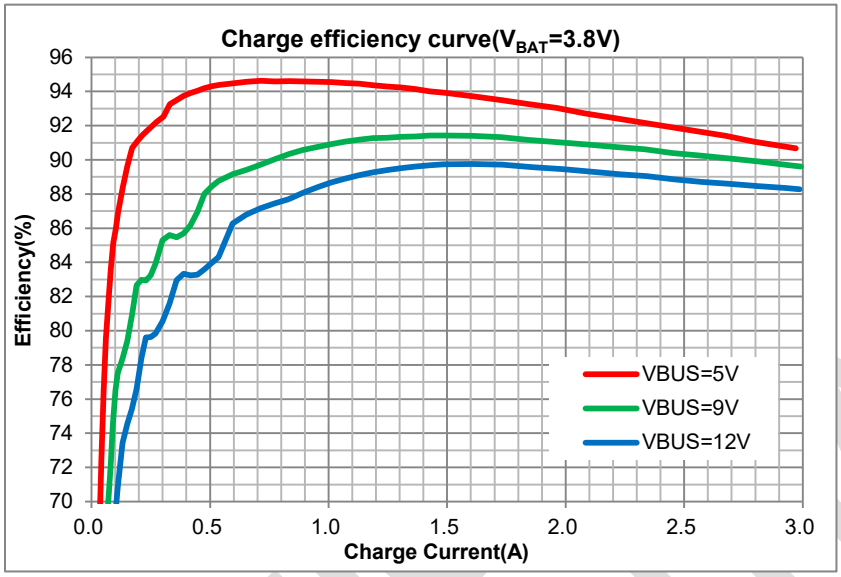



**Chart8** Charging efficiency at VBAT=3.8V

## 2.9 OTG efficiency

Test condition: $V_{BAT}$=3.8V/3.2V, $V_{OTG\_REG}$=5.15V, PFM enable/disable, measure boost mode efficiency.

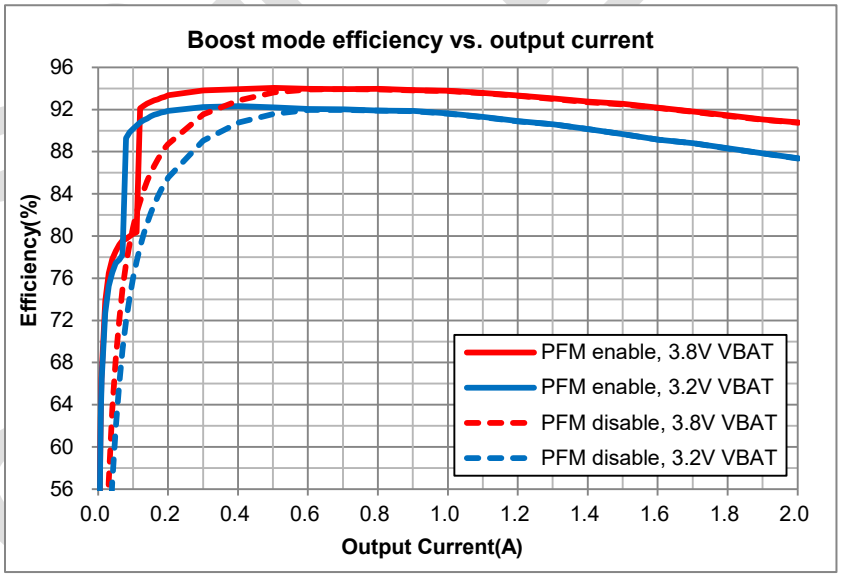


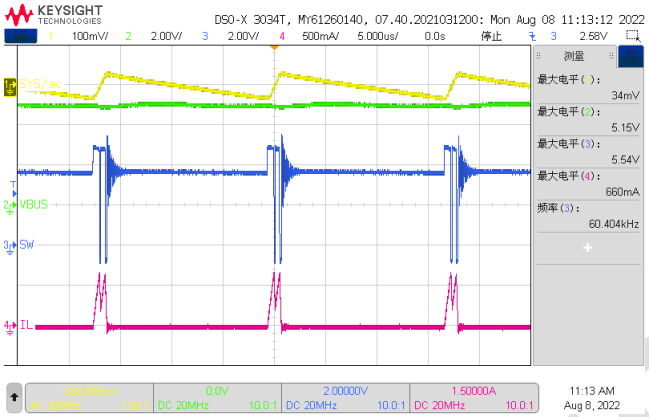

**Chart9** OTG at PMID=5.15V

## 2.10 Steady state operation

### 2.10.1 Charge mode

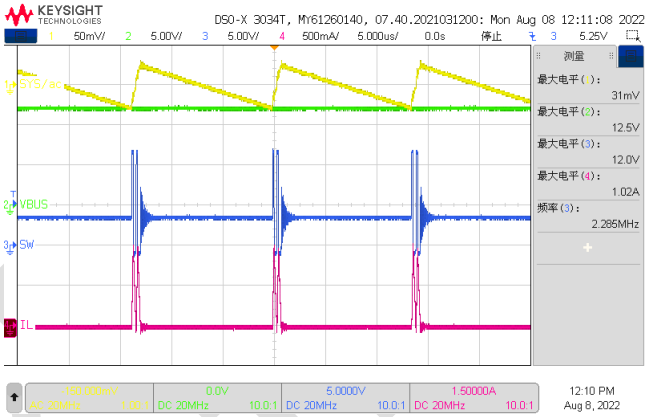
#### A. Trickle charge

Test condition: VBUS=5V/12V, VBAT=0V, charge enable.




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-1 VBUS=5V

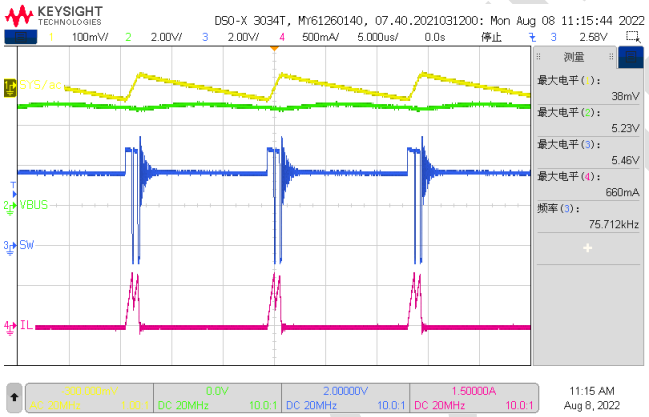



CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-2 VBUS=12V

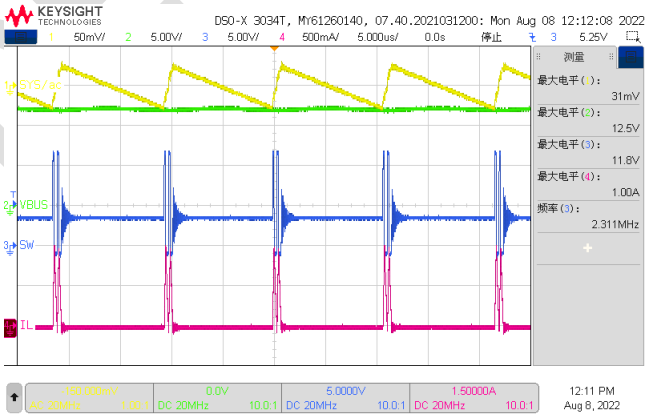
#### B. Pre-charge charge

Test condition: $V_{BUS}$=5V/12V, $V_{BAT}$=2.3V, $I_{PRECHG}$=40mA, charge enable.




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-3 VBUS=5V

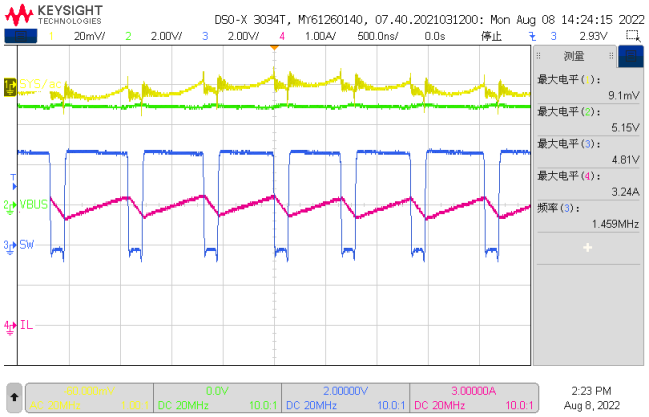



CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-4 VBUS=12V

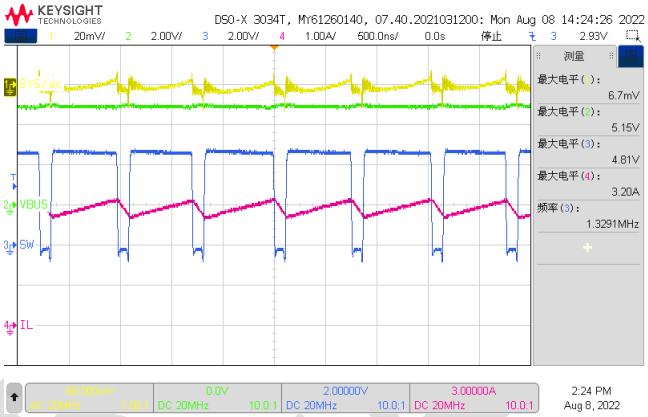
### C. Fast charge

Test condition: $V_{BUS}$=5V, $V_{REG}$ set to 4.624V, $V_{BAT}$=3.2V/3.8V, $I_{CHG\_SET}$=3000mA, charge enable.




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

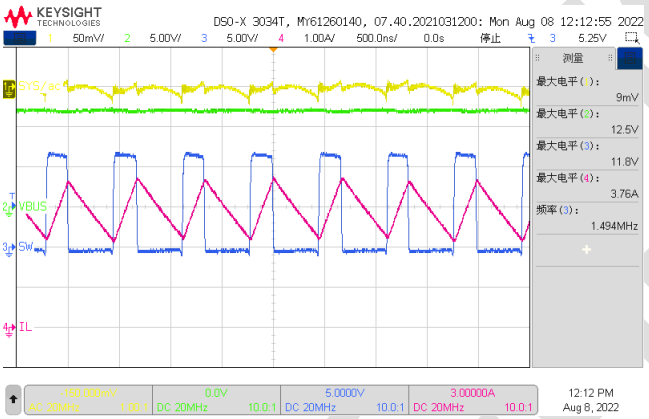
Fig-5 VBAT=3.2V




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

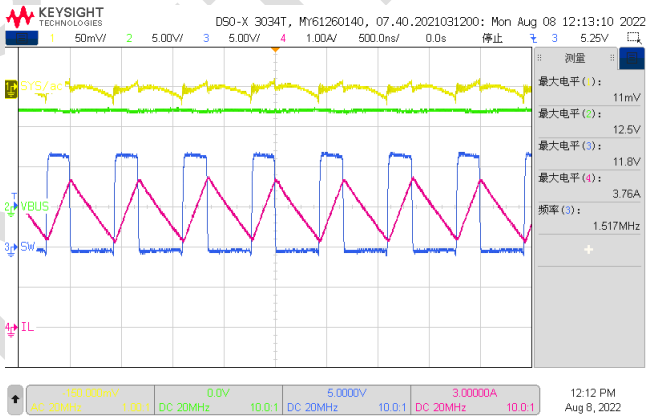
Fig-6 VBAT=3.8V

Test condition: $V_{BUS}$=12V, $V_{REG}$ set to 4.624V, $V_{BAT}$=3.2V/3.8V, $I_{CHG\_SET}$=3000mA, charge enable.




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-7 VBAT=3.2V

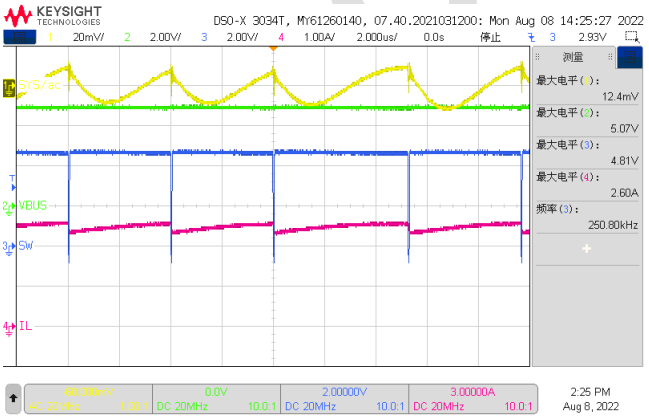



CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-8 VBAT=3.8V

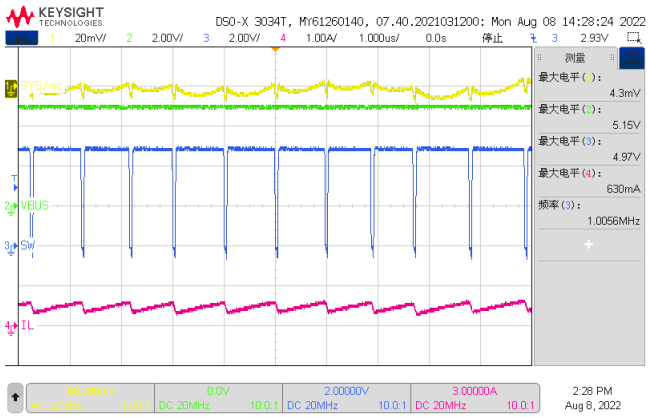
### D. Constant voltage charge

Test condition: $V_{BUS}$=5V, $V_{BAT\_REG}$=4.624V, $I_{CHG}$=3000mA, constant voltage charge




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

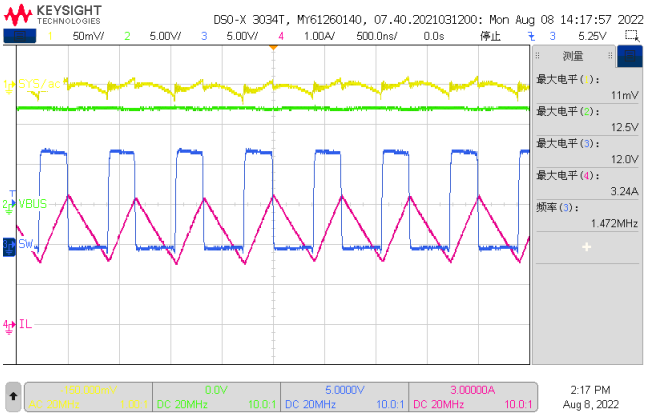
Fig-9 $I_{CHG}$=2.5A




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

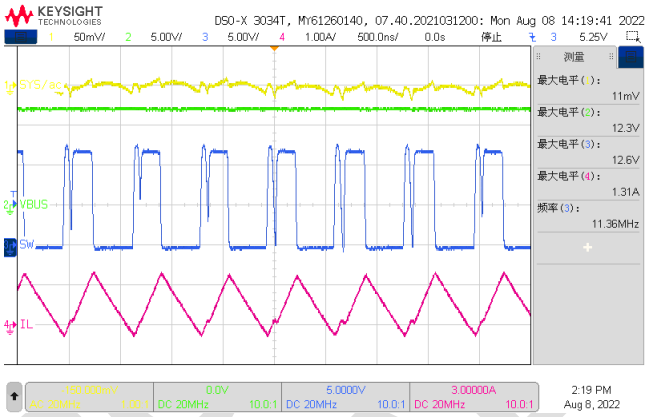
Fig-10 $I_{CHG}$=0.5A

Test condition: $V_{BUS}$=12V, $V_{BAT\_REG}$=4.624V, $I_{CHG}$=3000mA, constant voltage charge




CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-11 $I_{CHG}$=2.5A

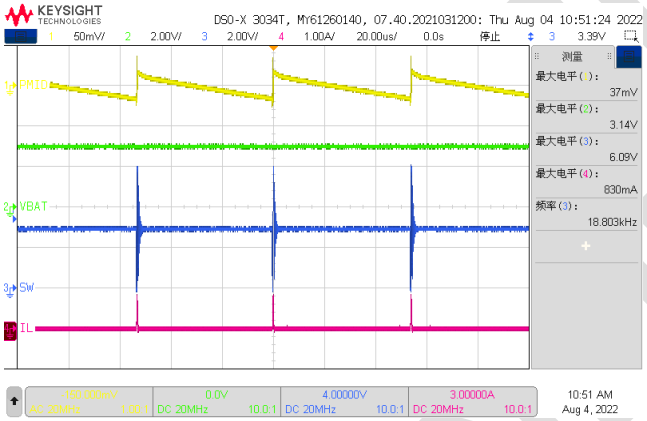



CH1-VSYS/ac, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-12 $I_{CHG}$=0.5A

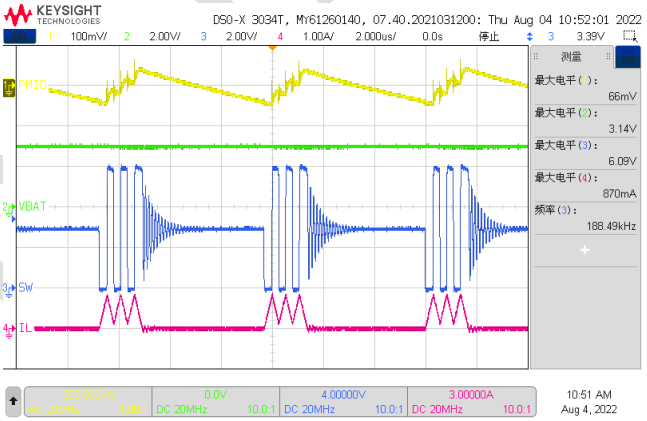
### 2.10.2 Boost mode

Test condition: OTG mode, $V_{BAT}$=3V.



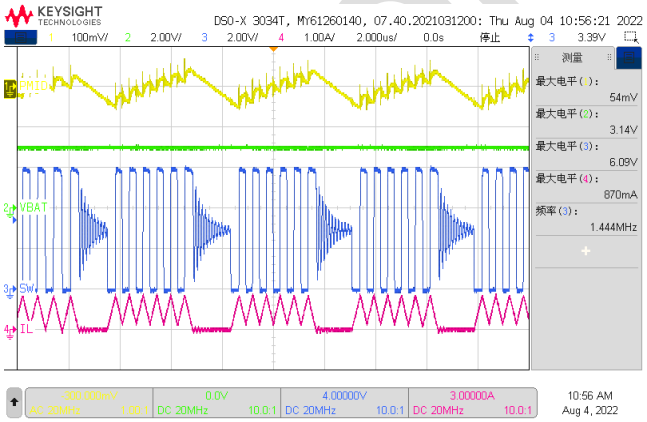

CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-13 No load.



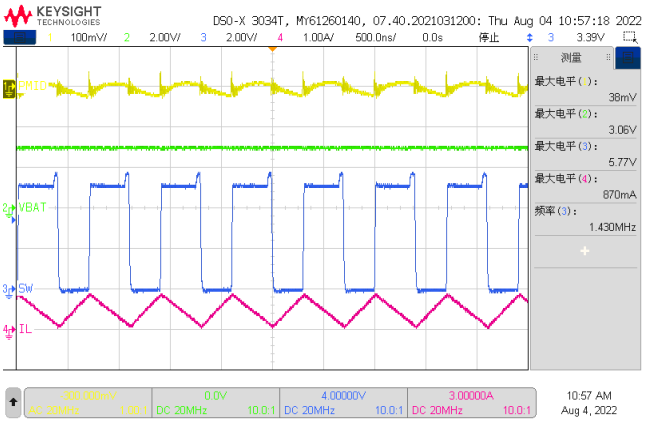

CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-14 $I_{LOAD\_OTG}$=0.05A.




CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

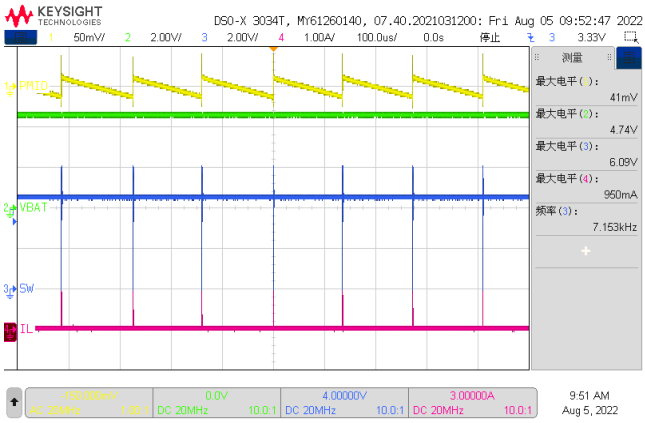
Fig-15 $I_{LOAD\_OTG}$=0.15A.




CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

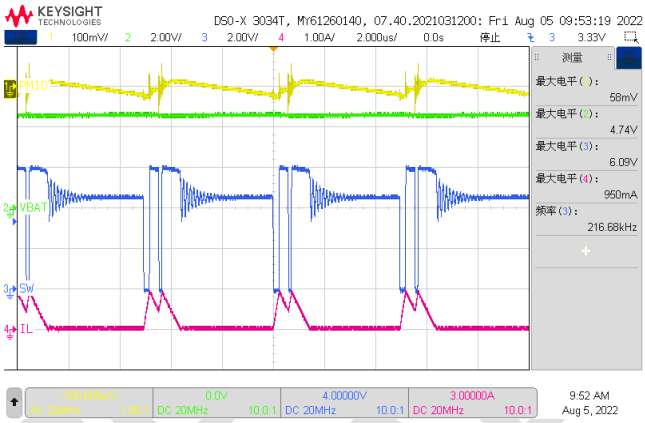
Fig-16 $I_{LOAD\_OTG}$=0.25A.

Test condition: OTG mode, $V_{BAT}$=4.6V.



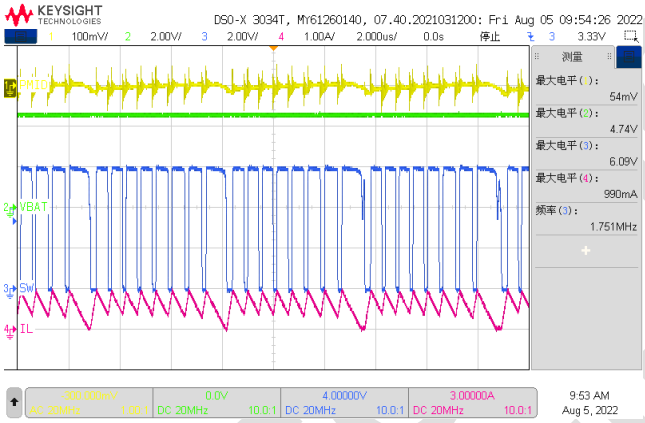

CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-17 No load.



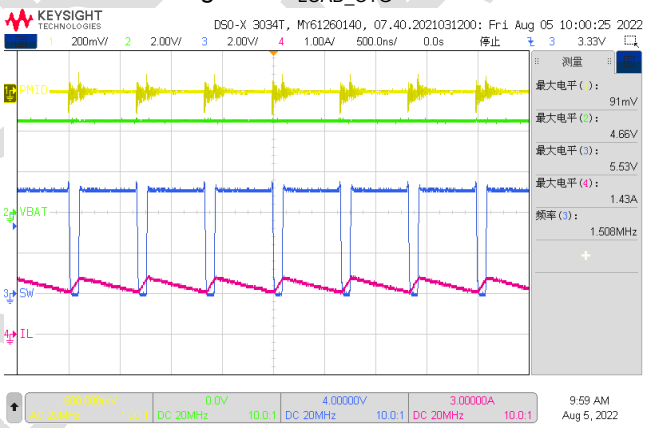

CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-18 $I_{LOAD\_OTG}$=0.1A.




CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-19 $I_{LOAD\_OTG}$=0.4A.



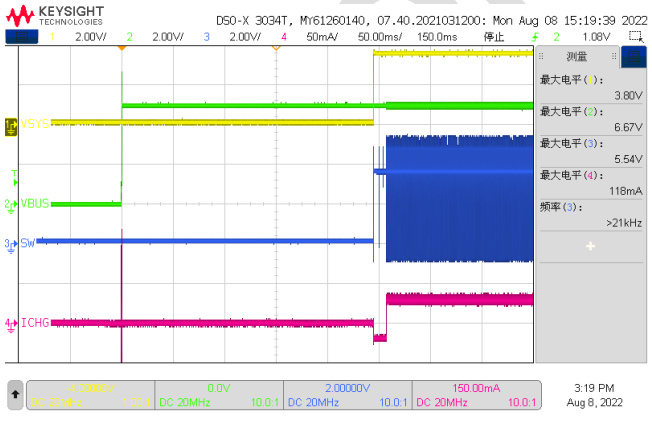

CH1-VOTG/ac, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-20 $I_{LOAD\_OTG}$=1A.

## 2.11 Transient test

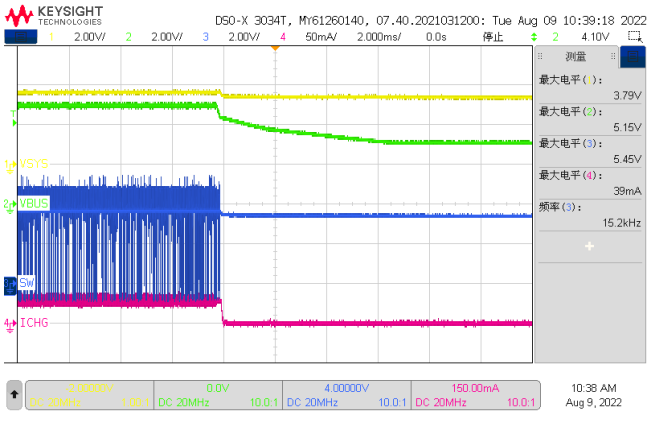
### 2.11.1 Adaptor plug in/out with battery

Test condition: $V_{BUS}$=5V, PSEL=Low, registers default setting, plug in/out adaptor at deferent battery voltage.



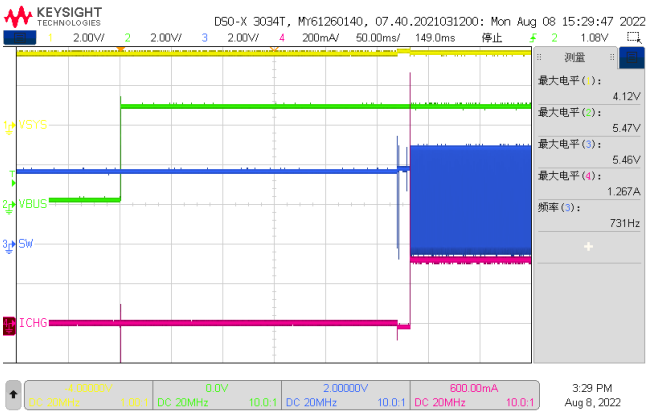

CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-21 Plug in 5V VBUS at $V_{BAT}$=1.5V.



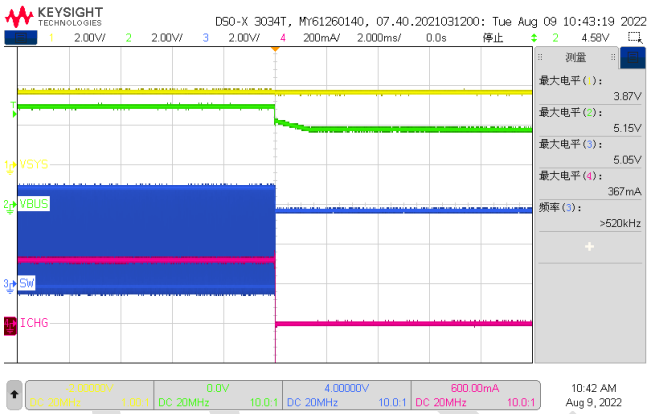

CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-22 Plug out 5V VBUS at $V_{BAT}$=1.5V.




CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

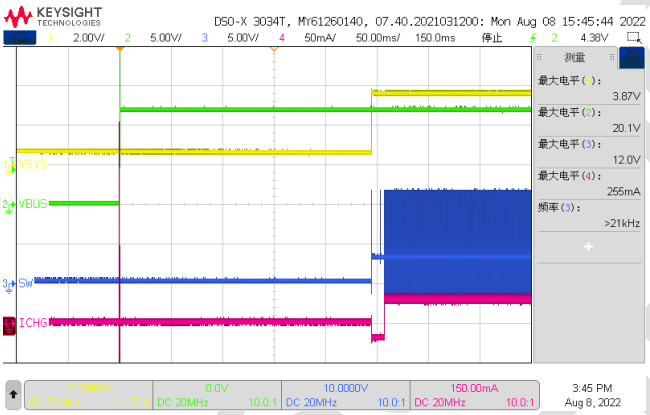
Fig-23 Plug in 5V VBUS at $V_{BAT}$=3.8V.




CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

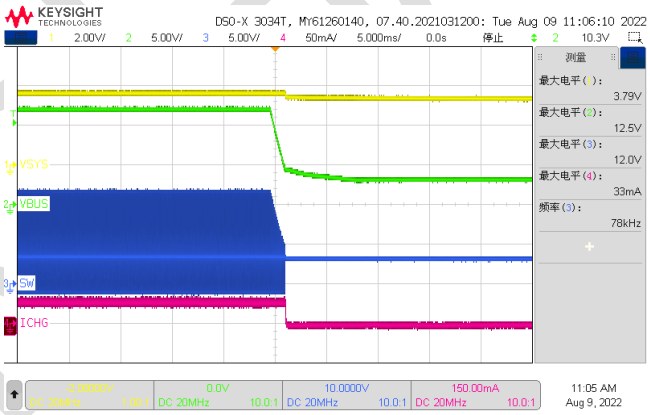
Fig-24 Plug out 5V VBUS at $V_{BAT}$=3.8V.

Test condition: $V_{BUS}$=12V, PSEL=Low, registers default setting, plug in/out adaptor at deferent battery voltage.



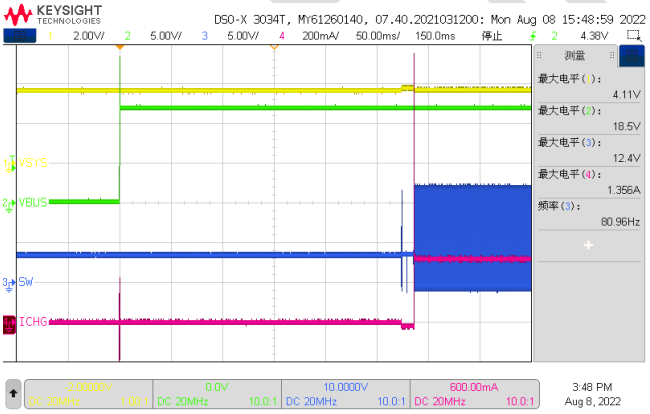

CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-25 Plug in 12V VBUS at $V_{BAT}$=1.5V.



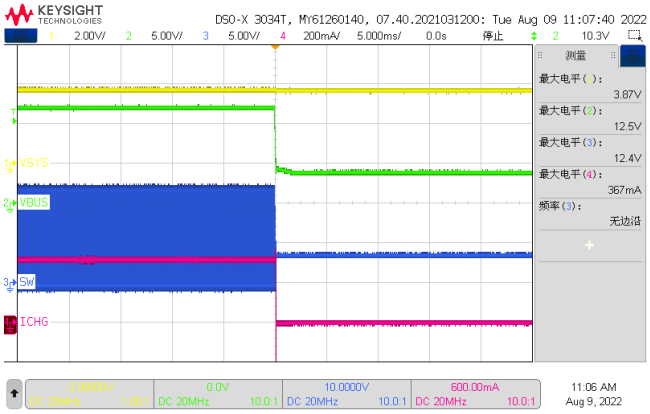

CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-26 Plug out 12V VBUS at $V_{BAT}$=1.5V.




CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-27 Plug in 12V VBUS at $V_{BAT}$=3.8V.

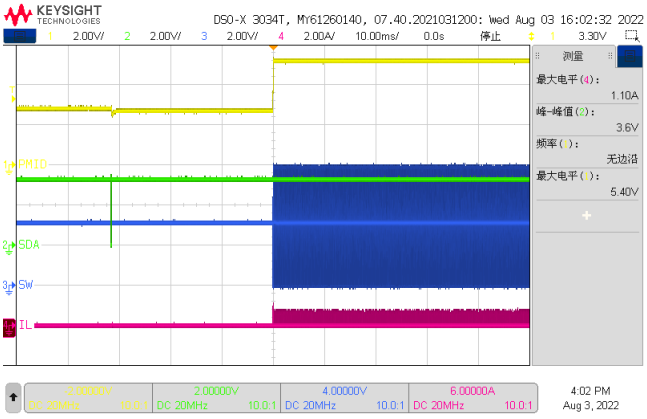



CH1-VSYS, CH2-VBUS, CH3-SW, CH4-$I_{CHG}$

Fig-28 Plug out 12V VBUS at $V_{BAT}$=3.8V.

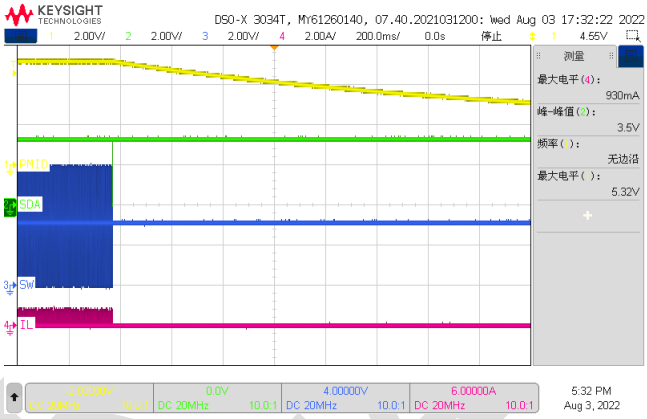
### 2.11.2 Enter/exit OTG mode

Test condition: $V_{BAT}$=3.2V, enter OTG mode with different load.



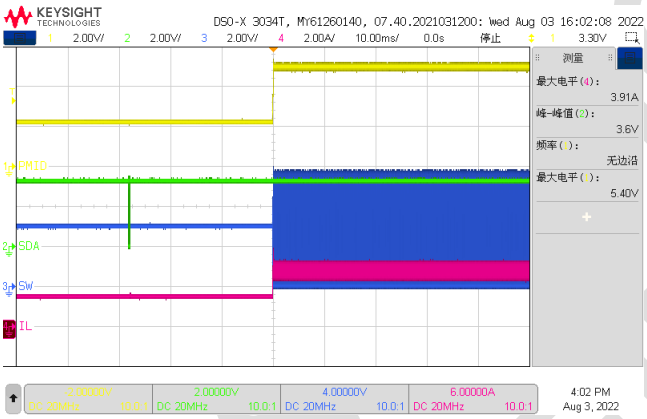

CH1-PMID, CH2-SDA, CH3-SW, CH4-$I_L$

Fig-29 Enter OTG mode, no load.



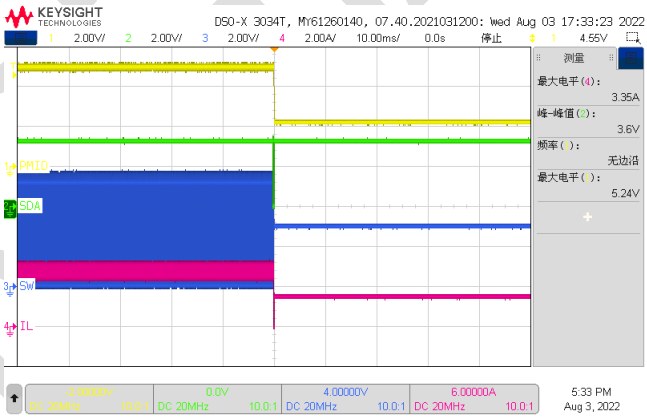

CH1-PMID, CH2-SDA, CH3-SW, CH4-$I_L$

Fig-30 Exit OTG mode, no load.




CH1-PMID, CH2-SDA, CH3-SW, CH4-$I_L$

Fig-31 Enter OTG mode, 1.5A CC load.

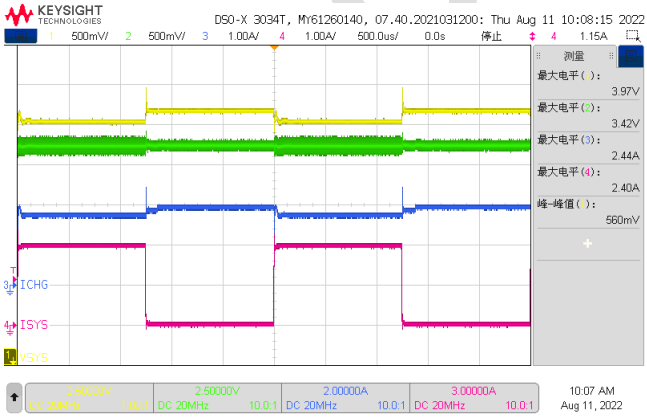



CH1-PMID, CH2-SDA, CH3-SW, CH4-$I_L$

Fig-32 Exit OTG mode, 1.5A CC load.

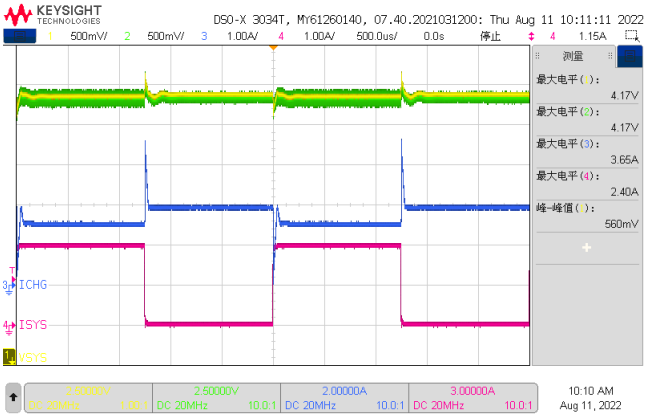
### 2.11.3 Dynamic system load

Test condition: $V_{BUS}$=5V, $V_{BAT}$=3.2V/3.8V, $I_{CHG\_SET}$=1980mA, $I_{INDPM}$=3200mA, add dynamic load current on SYS, $I_{SYS}$=0A-2A-0A(400Hz, SR=10A/μs).




CH1-VSYS, CH2-VBAT, CH3-ICHG, CH4-ISYS

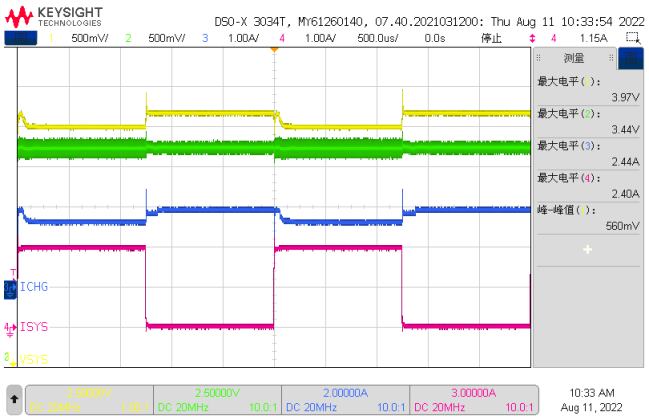
Fig-33 $V_{BAT}$=3.2V.




CH1-VSYS, CH2-VBAT, CH3-ICHG, CH4-ISYS

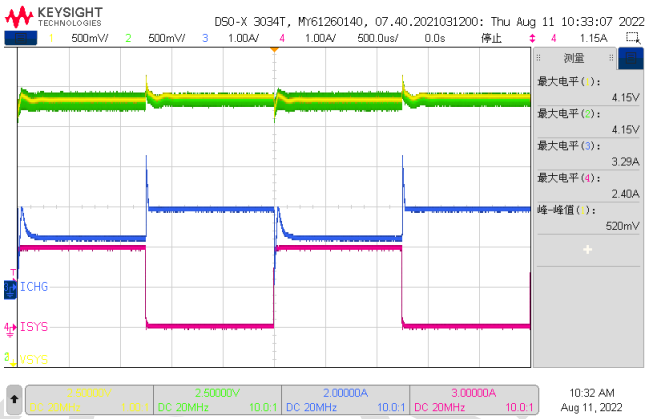
Fig-34 $V_{BAT}$=3.8V.

Test condition: $V_{BUS}$=12V, $V_{BAT}$=3.2V/3.8V, $I_{CHG\_SET}$=1980mA, $I_{INDPM}$=3200mA, add dynamic load current on SYS, $I_{SYS}$=0A-2A-0A(400Hz, SR=10A/μs).




CH1-VSYS, CH2-VBAT, CH3-ICHG, CH4-ISYS

Fig-35 $V_{BAT}$=3.2V.

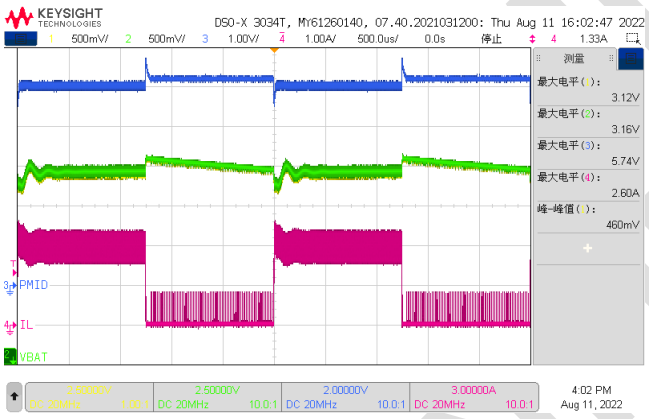



CH1-VSYS, CH2-VBAT, CH3-ICHG, CH4-ISYS

Fig-36 $V_{BAT}$=3.8V.

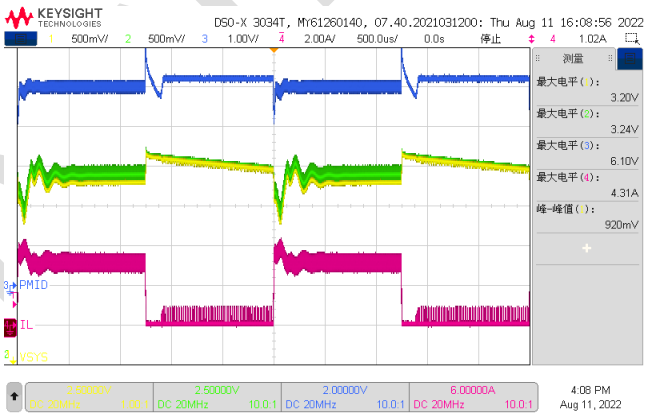
### 2.11.4 Load transient in OTG mode

Test condition: OTG mode, short VBUS, $V_{BAT}$=3V/4.6V, $I_{OTG}$=0A-1A-0A/0A-1.5A-0A (400Hz, SR=10A/μs).



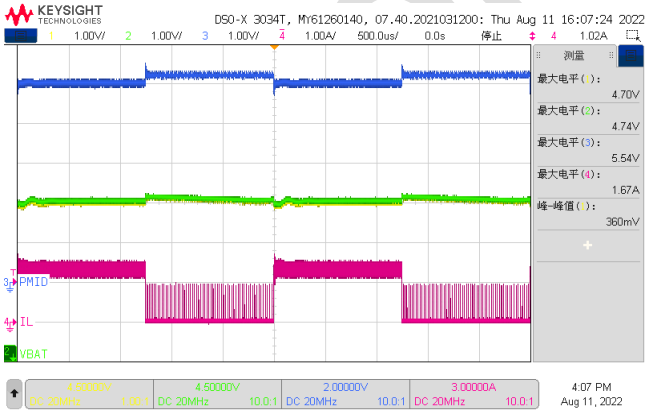

CH1-VSYS, CH2-VBAT, CH3-PMID, CH4-IL

Fig-37 $V_{BAT}$=3V, $I_{OTG}$=0A-1A-0A.



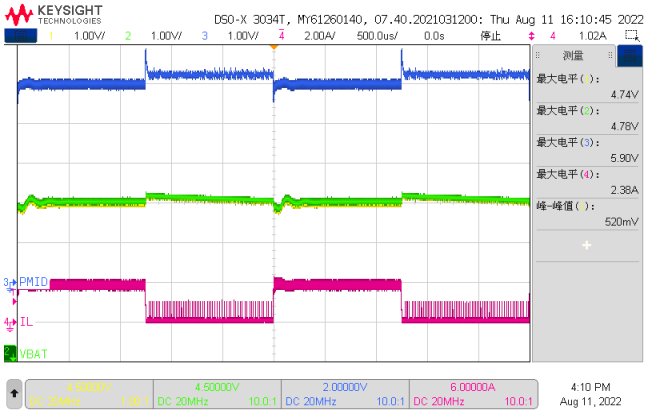

CH1-VSYS, CH2-VBAT, CH3-PMID, CH4-IL

Fig-38 $V_{BAT}$=3V, $I_{OTG}$=0A-1.5A-0A.




CH1-VSYS, CH2-VBAT, CH3-PMID, CH4-IL

Fig-39 $V_{BAT}$=4.6V, $I_{OTG}$=0A-1A-0A.



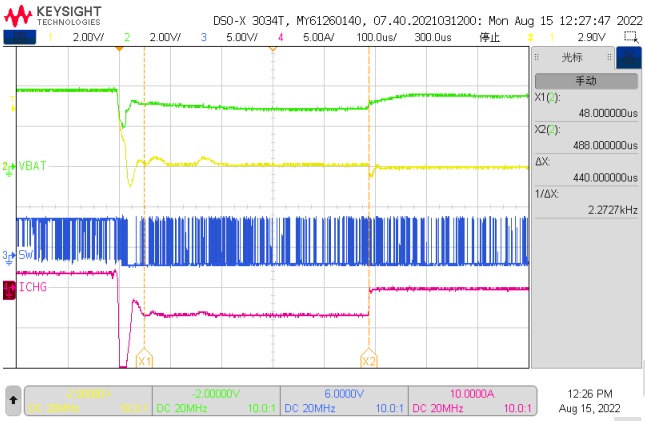

CH1-VSYS, CH2-VBAT, CH3-PMID, CH4-IL

Fig-40 $V_{BAT}$=4.6V, $I_{OTG}$=0A-1.5A-0A.

## 2.12 Reliability test

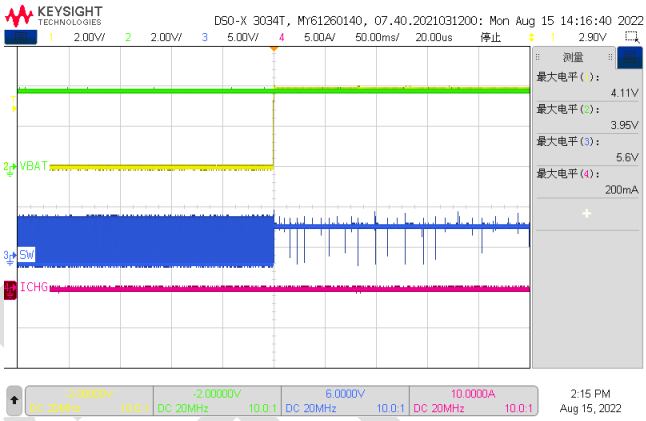
### 2.12.1 System SCP

Test condition: $V_{BUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG\_SET}$=1980mA, charge enable, BAT power supply current limit is 10A, short system to GND then release.




CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-41 Short system to GND.

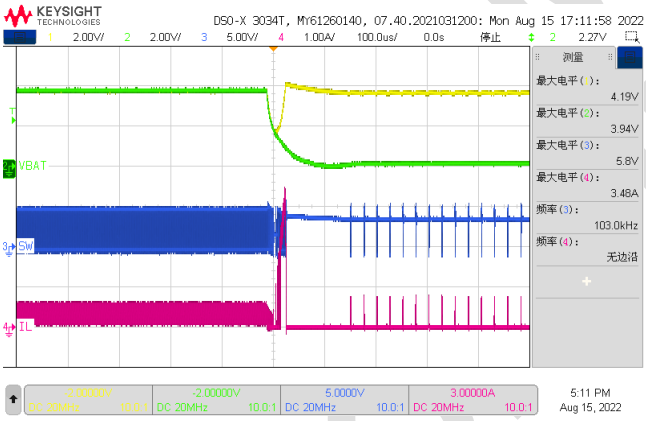



CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-42 Recovery from system short.

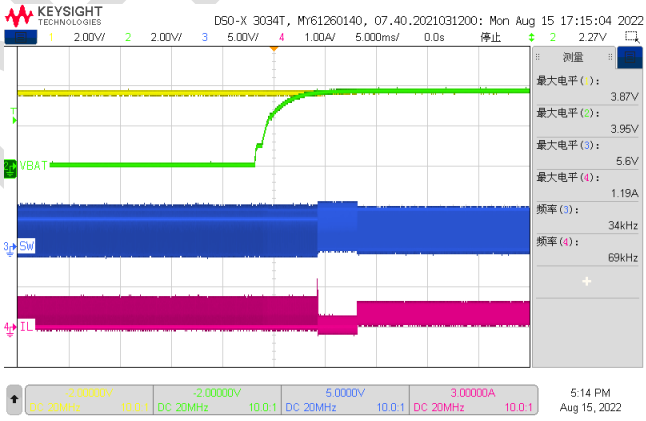
### 2.12.2 Battery SCP

Test condition: $V_{BUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG\_SET}$=330mA, charge enable, short battery to GND, then release.




CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-43 Short battery to GND.

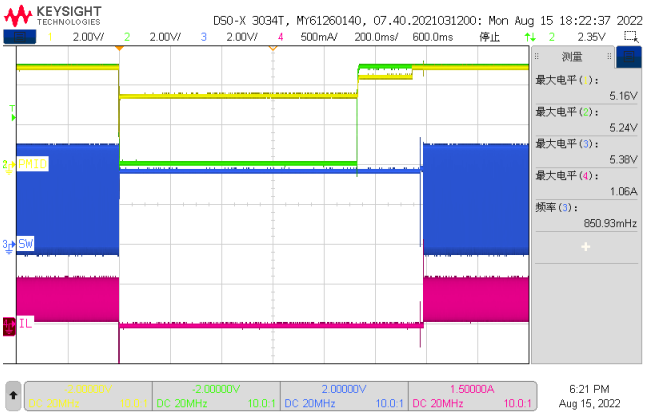



CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_L$

Fig-44 Recovery from battery short.

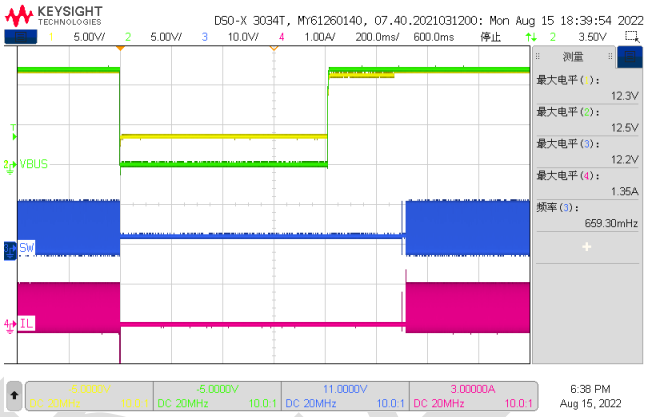
### 2.12.3 VBUS SCP

Test condition: $V_{BUS}$=5V/12V, $V_{BAT}$=3.8V, $I_{CHG\_SET}$=330mA, short VBUS to GND, then release.




CH1-PMID, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-45 VBUS=5V.

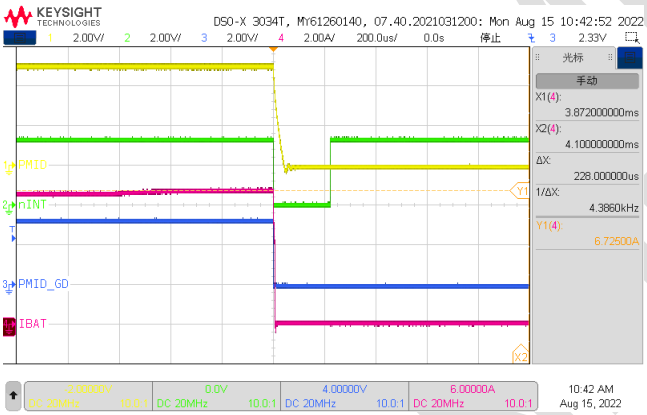



CH1-PMID, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-46 VBUS=12V.

### 2.12.4 PMID OCP&SCP in OTG mode

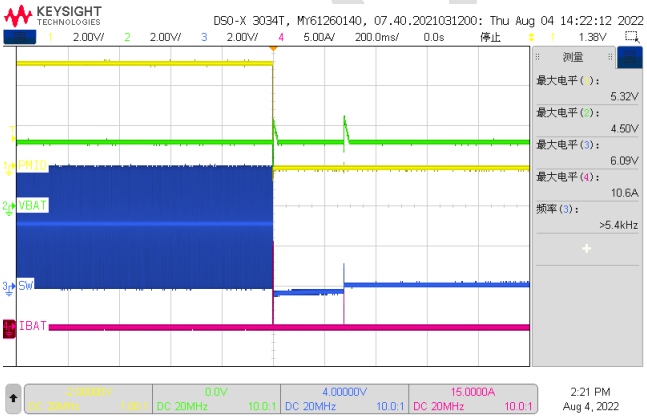
Test condition: OTG mode, $V_{BAT}$=3.8V, ISYS=5A, increase IPMID to trigger OCP.




CH1-VOTG, CH2-nINT, CH3-PMID_GD, CH4-$I_{DISCHG}$

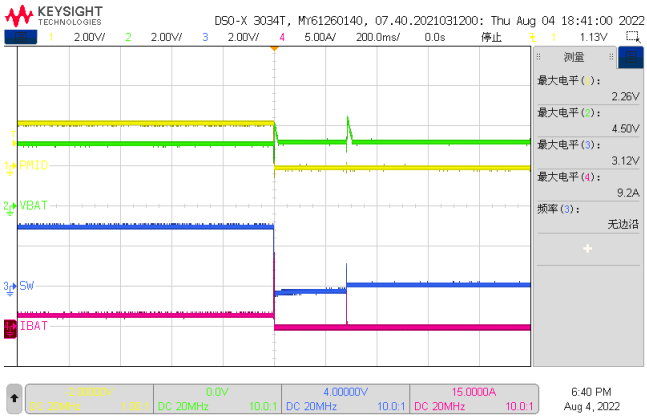
Fig-47 Increase IPMID.

Test condition: OTG mode, VBAT=3.2V, then short PMID to GND




CH1-PMID, CH2-VBAT, CH3-SW, CH4-$I_{DISCHG}$

Fig-48 $I_{OTG}$=0A.

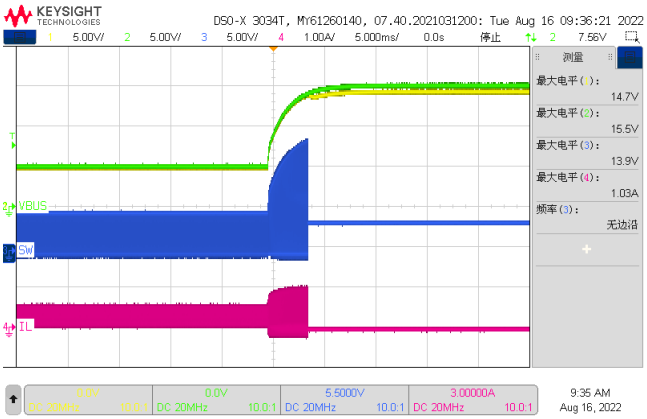



CH1-PMID, CH2-VBAT, CH3-SW, CH4-$I_{DISCHG}$

Fig-49 $I_{OTG}$=1.5A.

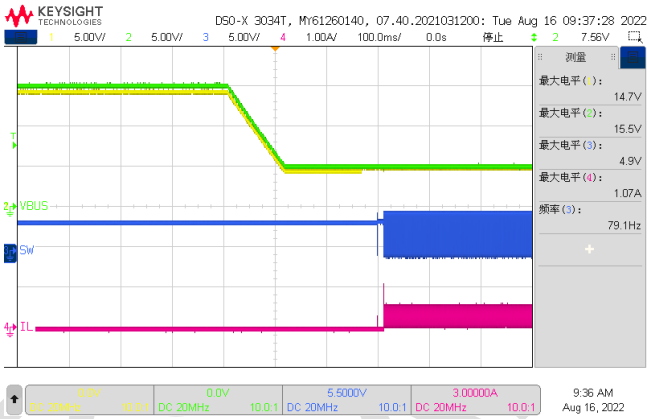
### 2.12.5 VBUS OVP

Test condition: OVP set to 14V, $V_{BUS}$=5V, $V_{BAT}$=3.8V, charge enable, $V_{BUS}$ ramp to 15V.




CH1-PMID, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-50 $V_{BUS}$ increase from 5V to 15V.

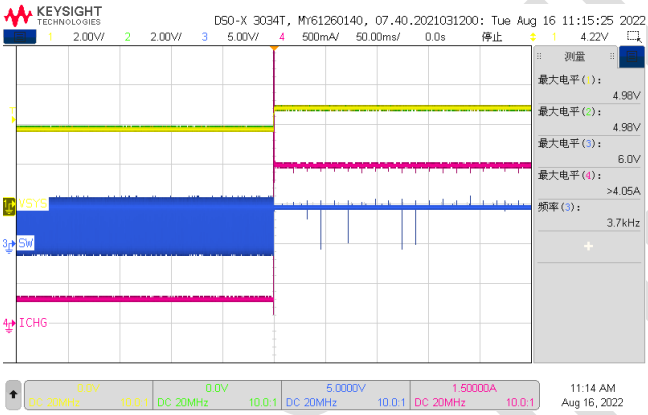



CH1-PMID, CH2-VBUS, CH3-SW, CH4-$I_L$

Fig-51 $V_{BUS}$ decrease from 15V to 5V.

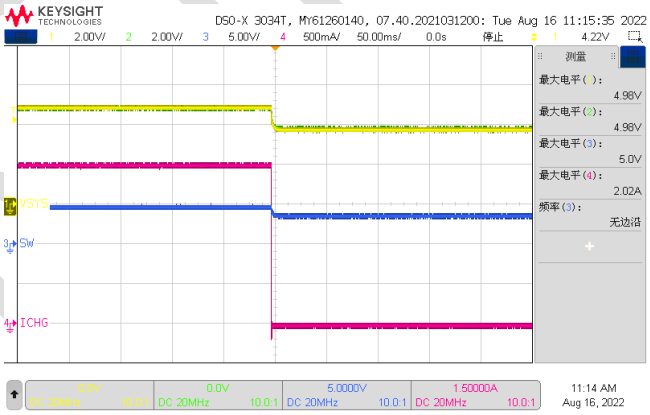
### 2.12.6 VSYS OVP

Test condition: $V_{BUS}$=5V, $V_{BAT}$=3.8V, charge enable, $I_{SYS}$=0A, force a 5V external power supply on system.




CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-52 Plug in 5V power supply on SYS.

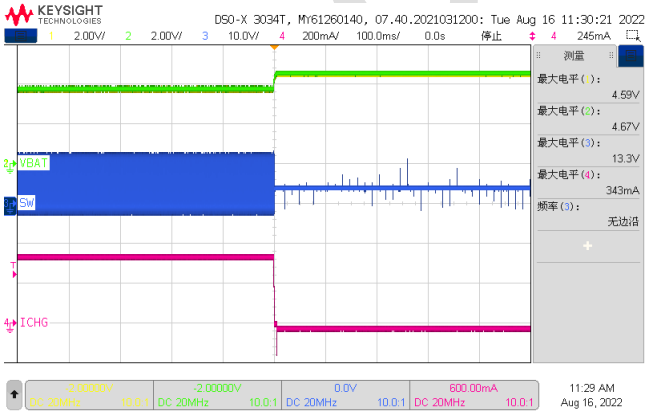



CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-53 Plug out 5V power supply on SYS.

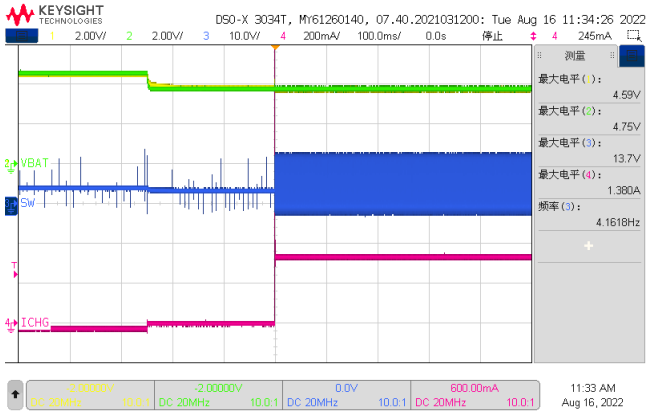
### 2.12.7 VBAT OVP

Test condition: $V_{BUS}$=12V, $V_{BAT}$=3.8V, charge enable, $V_{BAT\_REG}$=4.208V, $V_{BAT}$ ramp to 4.6V.




CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-54 $V_{BAT}$ increase from 3.8V to 4.6V.

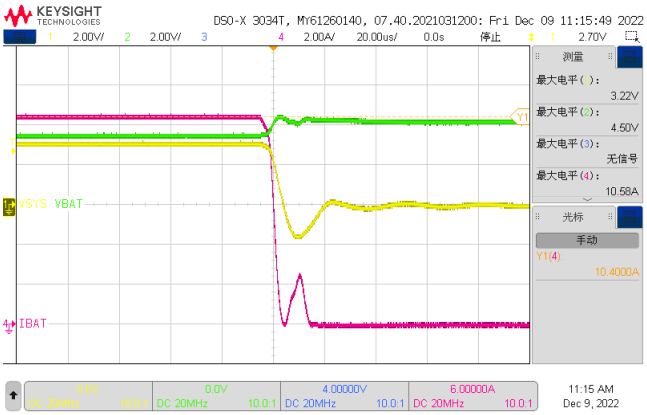



CH1-VSYS, CH2-VBAT, CH3-SW, CH4-$I_{CHG}$

Fig-55 $V_{BAT}$ decrease from 4.6V to 3.8V.

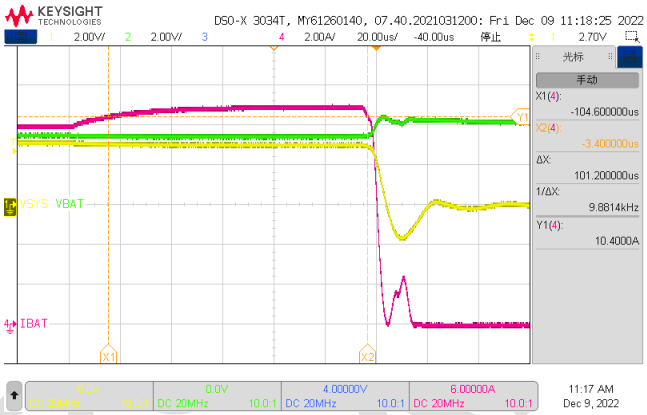
### 2.12.8 BATFET OCP

Test condition: no VBUS, $V_{BAT}$=3.8V, BATFET on, add CC mode E-load on system and increase load by 0.1A/1A step.




CH1-VSYS, CH2-VBAT, CH4-$I_{DISCHG}$

Fig-56 Increase $I_{SYS}$ to 10.45A by 0.1A step.




CH1-VSYS, CH2-VBAT, CH4-$I_{DISCHG}$

Fig-57 Increase $I_{SYS}$ to 11A by 1A step.